A Cutting-Edge Digital Gate Drive Technology for High-Efficiency Power Semiconductor Operation

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Abstract

In pursuit of carbon neutrality by 2050, the presence of power electronics equipment is growing, driven by the expansion of renewable energy and other factors. In power electronics equipment, the power loss (switching energy loss) and electromagnetic noise generated by the switching operation of power devices have a trade-off relationship. Digital gate drive technology is drawing attention as a power-device driving technique to improve this trade-off relationship.

In this work, through joint research with the University of Tokyo, the authors proposed a drive method that changes the signal strength for driving power devices at optimal timing using a general-purpose gate driver integrated circuit (IC). Compared with conventional drive methods, the proposed drive method achieved a reduction in turn-on switching energy loss of 25% and 18% at load currents of 50 A and 100 A, respectively. The application of the proposed digital gate drive technology is expected to contribute to further energy savings in power electronics equipment.

1. Introduction

Digital gate drive technology that changes the drive signal strength in multiple steps during the switching operation of power devices is drawing attention. This technology makes it possible to improve the trade-off relationship between switching loss and electromagnetic noise in power modules. By optimizing the timing for varying the drive signal strength in accordance with operating conditions such as load current I_L and temperature, the technology contributes to energy savings in power electronics equipment[(1)]. Figure 1 shows a method for determining the timings t_1 and t_2 at which to change the drive signal strength[(1) (2) (3)] with respect to the gate-emitter voltage V_{GE} and collector current Ic during turn-on operation of the power module. In this study, the authors propose a novel timing determination method that changes the drive signal strength to “strong, weak (high impedance), and strong” and determines the timings t_1 and t_2 at which to change the drive signal strength. Furthermore, the authors verified the validity of the proposed method based on the evaluation results using a general-purpose gate driver integrated circuit (IC).

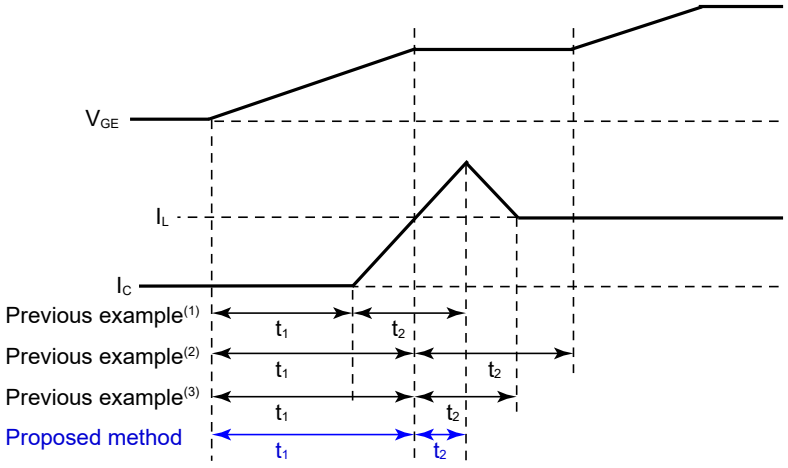
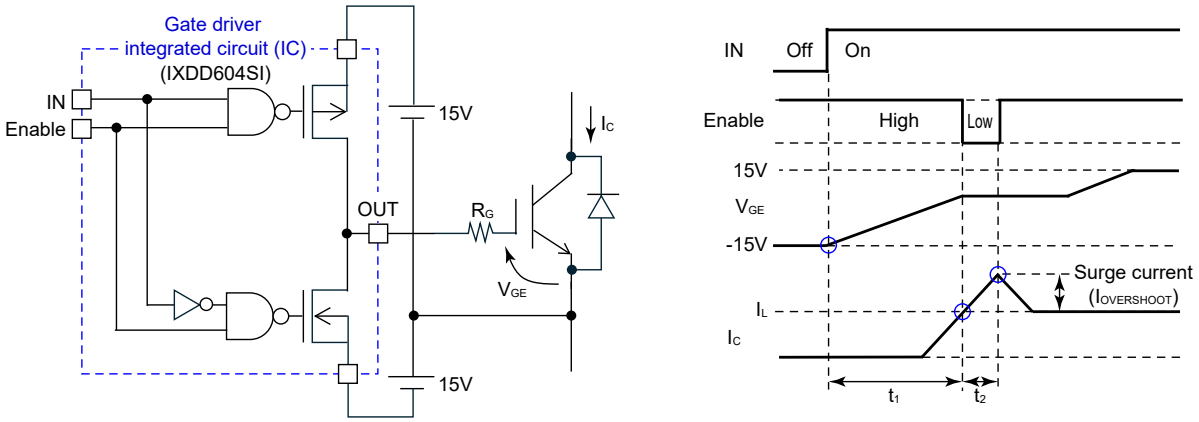


Fig. 1 Various methods for determining t_1 and t_2 at turn-on

2. Proposed Method for Determining Optimal Drive Timing

Figure 2 shows the circuit diagram and timing chart of the proposed method. The proposed method uses a gate driver integrated circuit (IC) which has Enable function (IXDD604SI). The timing t_1 and t_2 in the timing chart are controlled by the input signal IN and the Enable signal. When the Enable signal is low, the output OUT becomes high impedance. In the proposed method, t_1 is the period from the rising edge of V_{GE} to the timing when I_C reaches the load current I_L, and t_2 is the period from the timing at which I_C reaches the load current I_L to the timing at which I_C reaches its peak value. The values of t_1 and t_2 change as the operating conditions of the power module and they are calculated from the measured V_{GE} and I_C waveforms.



(a) Circuit diagram (b) Timing chart

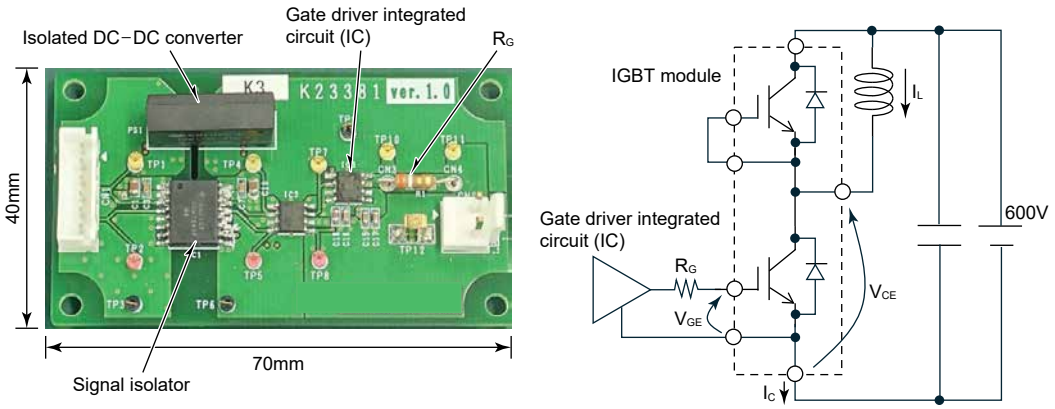
Fig. 2 Circuit diagram and timing chart of the proposed method

The loss reduction rate in the proposed method is defined by Equation (1), where $E_{LOSS,\ DGD}$ denotes the switching energy loss in the proposed method, and $E_{LOSS,\ CONV}$ denotes the switching energy loss in the conventional gate drive circuits (hereafter referred to as the “conventional method”). $E_{LOSS,\ DGD}$ is obtained with the measurement results. $E_{LOSS,\ CONV}$, on the other hand, is calculated using the trade-off curve, that is measured by varying the gate resistance R_G with conventional method, between energy loss E_{LOSS} and surge current $I_{OVERSHOOT}$.

$$\text{Loss reduction rate} = \frac{E_{LOSS,\ CONV} - E_{LOSS,\ DGD}}{E_{LOSS,\ CONV}} \times 100 \quad \cdots\cdots (1)$$

3. Evaluation Method

Figure 3 shows the gate driver board and the circuit diagram for switching evaluation. The gate driver board is equipped with a signal isolator and an isolated DC-DC converter. An Insulated Gate Bipolar Transistor (IGBT) module (CM100DY-24T, rating: 1,200 V, 100 A) was used as a device under test. In this study, t_1 and t_2 were measured using the determination methods of the proposed method and the conventional method, as well as the previous examples[1][2][3] respectively. In the proposed method, t_1 and t_2 were measured with 2,400 combinations at 2 ns intervals.

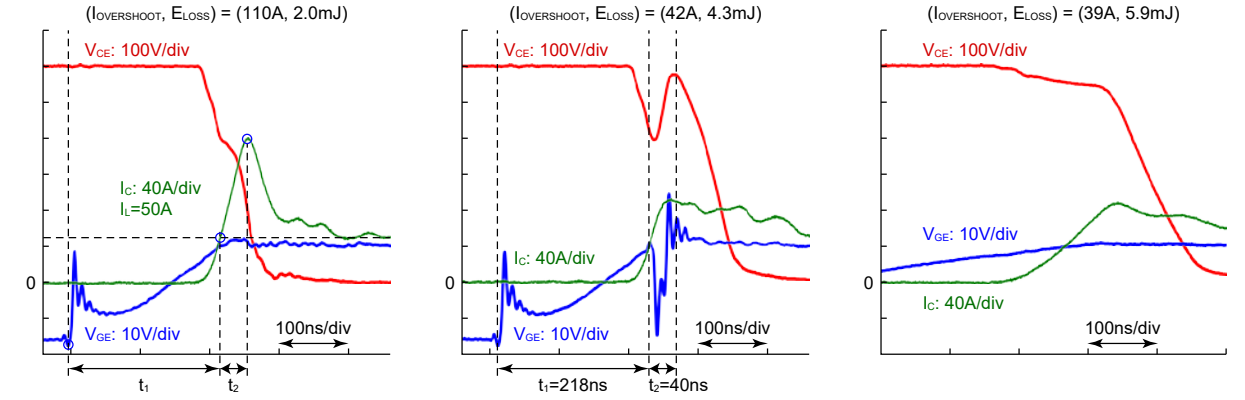


(a) Gate driver board (b) Switching evaluation circuit diagram

Fig. 3 Gate driver board and switching evaluation circuit diagram

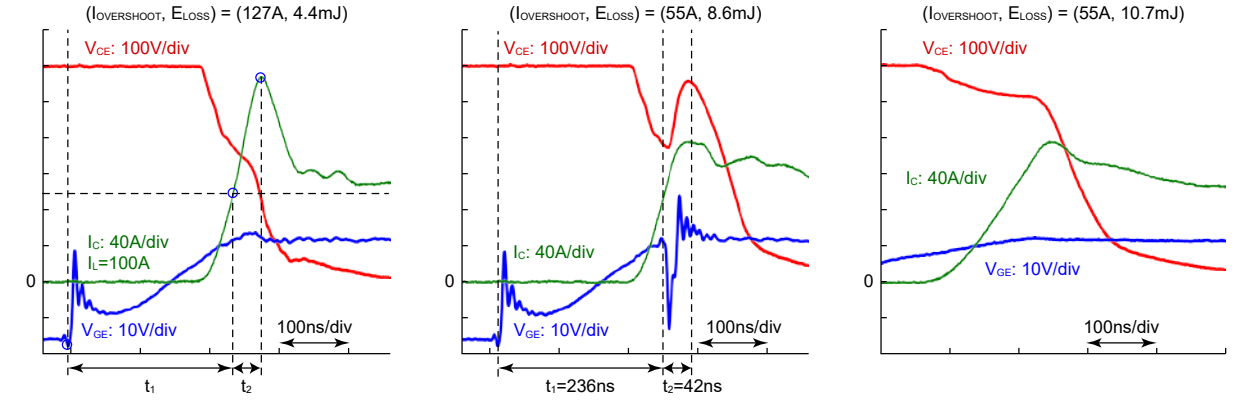
4. Evaluation Results

Figure 4 and Fig. 5 show the switching waveforms for the proposed method and the conventional method at load currents I_L =50 A and 100 A, respectively. For the proposed method, t_1 and t_2 were calculated from the switching waveform on condition that the gate resistance R_G of the conventional method was set to 3.9 Ω. The switching energy loss and surge current were obtained from these switching waveforms, and the loss reduction rate was compared.



(a) Conventional method Point A1 (R_G=3.9Ω) (b) Proposed method (c) Conventional method Point B1 (R_G=18Ω)

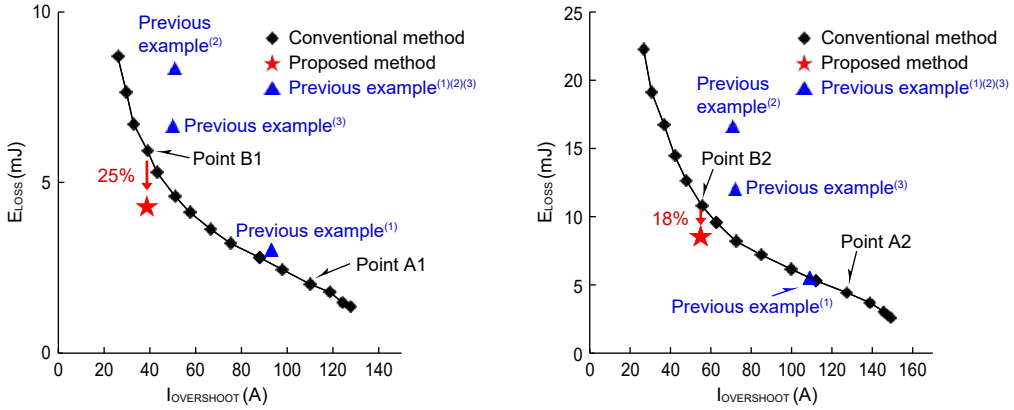
Fig. 4 Switching waveforms of the proposed method and the conventional method at I_L=50 A



(a) Conventional method Point A2 (R_G=3.9Ω) (b) Proposed method (c) Conventional method Point B2 (R_G=12Ω)

Fig. 5 Switching waveforms of the proposed method and the conventional method at I_L=100 A

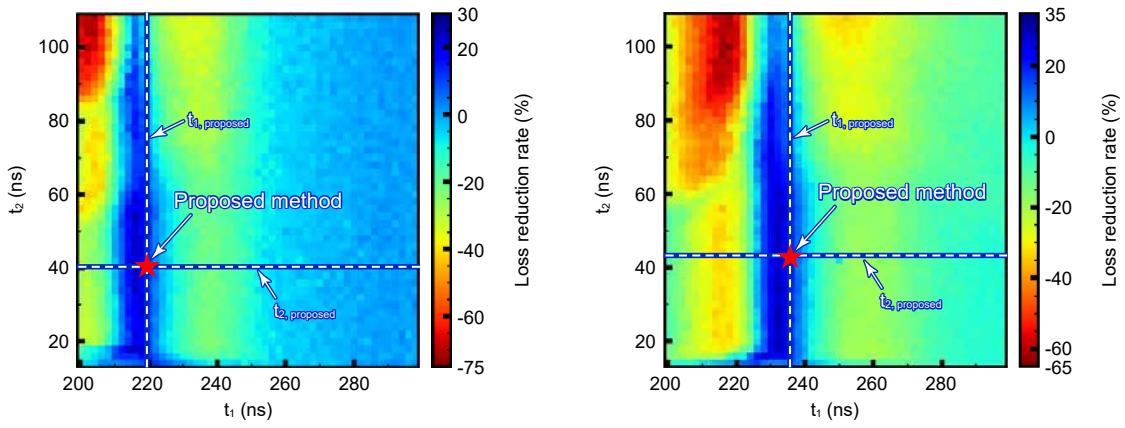
Figure 6 shows the evaluation results for the proposed method, the conventional method, and previous examples[1][2][3] of switching energy loss E_{LOSS} and surge current $I_{OVERSHOOT}$ at load currents I_L = 50 A and 100 A. With the proposed method, while maintaining the surge current $I_{OVERSHOOT}$ at about the same level as the conventional method, E_{LOSS} was reduced by 25% at load current I_L = 50 A, and 18% at I_L = 100 A, respectively. Note that E_{LOSS} in the previous examples[1][2][3] was higher than that in the conventional method when compared on condition that $I_{OVERSHOOT}$ matched that of the conventional method, indicating a deterioration in switching loss.



(a) I_L=50A (b) I_L=100A

Fig. 6 Evaluation results of switching loss E_{LOSS} and surge current $I_{OVERSHOOT}$

Figure 7 shows the dependence of the loss reduction rate on t_1 and t_2 at load current I_L = 50 A and 100 A. Optimizing t_1 is important because the loss reduction rate depends significantly on t_1 while the dependence on t_2 is small. With the proposed method, the authors were able to obtain the optimal value of t_1, which has a large impact on the loss reduction rate and achieved a higher loss reduction effect. Table 1 shows the evaluation results of the loss reduction rate at temperatures T_j of 25°C, 75°C, and 125°C for the proposed method and previous examples[1][2][3]. Even under conditions with temperatures T_j of 75°C and 125°C, the authors confirmed that the proposed method achieves a higher loss reduction effect than previous examples[1][2][3].



(a) Load current I_L=50A (b) Load current I_L=100A

Fig. 7 Dependence of loss reduction rate on t_1 and t_2

Table 1 Loss reduction rate of the proposed method and previous examples[1][2][3]

	I_L=50 A			I_L=100 A		
	T_j=25°C	T_j=75°C	T_j=125°C	T_j=25°C	T_j=75°C	T_j=125°C
Proposed method (%)	25	23	16	18	26	27
Previous example[1] (%)	-20	-10	-9	0	-2	-1
Previous example[2] (%)	-84	-64	-50	-95	-96	-70
Previous example[3] (%)	-43	-75	-64	-45	-78	-90

5. Conclusion

The authors proposed a novel method for digital gate drive technology to determine the timing for adjusting the strength of the drive signal. The proposed method achieved the maximum loss reduction effect, demonstrating its validity.

The authors will continue to develop the proposed method toward practical implementation, contributing to energy savings in power electronics equipment.

References

(1) Zhang, F., et al.: Advanced Active Gate Drive for Switching Performance Improvement and Overvoltage Protection of High-Power IGBTs, IEEE Transactions on Power Electronics, 33, No.5, 3802–3815 (2017)
(2) Camacho, P.A., et al.: A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory, IEEE Transactions on Industrial Electronics, 64, No.11, 9032–9042 (2017)
(3) Manuel, R., et al.: Implementation of Current-Source Gate Driver with Open-Loop Slope Shaping for SiC-MOSFETs, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 1–8 (2021)