Low Power Design of Real-Time Forward Error Correction Circuit Based on the Characteristics of State-of-the-Art Processes

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Abstract

In realizing a digital society, we cannot avoid the issues of increasing the speed of digital signal processing and lowering its power consumption. To simultaneously achieve these contradictory characteristics, it is important not only to make advances in digital signal processing technology and integration technology made possible by the miniaturization of semiconductor processes, but also to develop low-power digital design techniques that take into account the characteristics of systems and applications. This paper describes low-power design technology that applies advanced wafer manufacturing processes, using the development of error-correction circuits for large-capacity optical communications as an example. Circuit design with high feasibility was achieved by optimizing the code and circuit architecture based on physical synthesis results assuming process characteristics, and power reduction effectiveness exceeding 40% was obtained, relative to maximum operation, through circuit control taking into account characteristics in terms of equipment operation.

1. Introduction

Social transformation continues to move forward, based on digital technologies exemplified by Digital Transformation (DX). Increasing the capacity of digital signal processing, and reducing its power consumption, are perennial topics in the use of such digital technology. In the optical communication industry, systems exceeding 400Gbps are being introduced to cope with growing traffic demand, and R&D is being conducted to further increase speed to 800Gbps and beyond. The improvement in communication speed is largely due to developments in signal processing technology, including error-correction technology, and integration technology resulting from the miniaturization of semiconductor processes. Previously, progress has been made in increasing capacity through parallelization and improved operating frequencies, while also reducing power consumption through process miniaturization. However, in recent years, the improvement of operating frequency has reached its limit, and in order to achieve high-speed processing, there is no choice but to rely on parallel processing. Since the effect of reducing power consumption by process miniaturization is small compared to the increase in power consumption due to parallelization, it is becoming difficult to meet the power consumption requirements. In particular, since the power consumption of error-correction circuits accounts for a large proportion of the power consumption within the device, reducing the power consumption has become increasingly important in recent years. In this paper, we first outline the forward error correction code circuit that is the target of power saving, and then describe the power saving technology we have developed from the perspectives of circuit element implementation and algorithm processing.

2. Technical Trends of Forward Error Correction Codes for Optical Communications

In optical communication networks, Low-Density Parity-Check (LDPC) codes, which have excellent correction capabilities, are often used as forward error correction codes to achieve error-free, large-capacity transmission over long distances. LDPC codes were proposed by Gallager in the 1960s[(1)] and have recently been adopted in standards for satellite digital broadcasting and wireless communications. This section explains these LDPC codes.

2.1 LDPC codes

LDPC codes are codes defined by a sparse parity check matrix (many “0” s and few “1” s) and are known to achieve high error-correction performance. Figure 1 shows an example of a check matrix and its representation as a bipartite graph. With an LDPC code, errors are corrected by propagating beliefs using the connection relationships of the graph. The distinguishing features of this decoding processing are that it is suitable for parallel processing by hardware, and it enables circuit implementation with high throughput. However, LDPC codes with practical code length are connected irregularly due to the huge amount of Tanner graph wiring, and thus the difficulty of decoding circuit implementation is extremely high. Therefore, it is important to design check matrices with high error-correction performance and circuit feasibility.

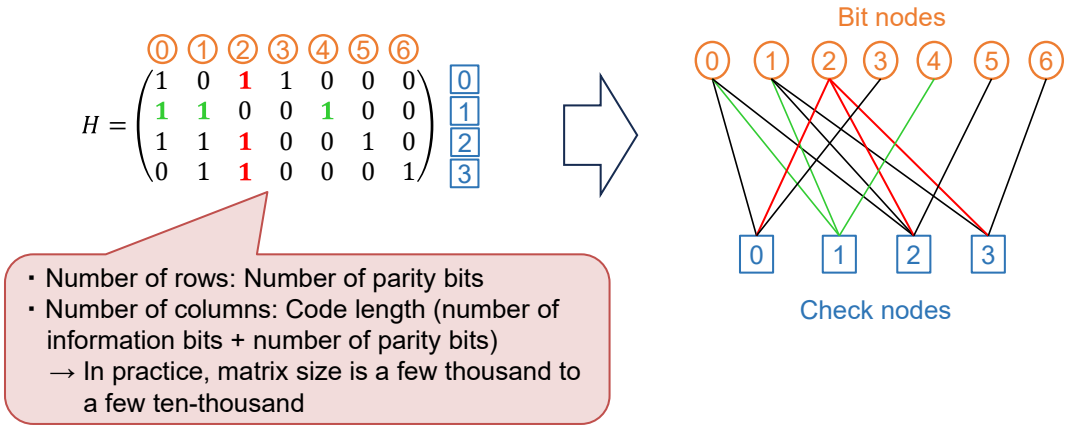

Fig. 1 Example of a parity check matrix and its Tanner graph

2.2 Quasi-Cyclic LDPC

Quasi-Cyclic (QC) LDPC codes are being considered as codes having both good error-correction performance and circuit implementability. With QC-LDPC codes, non-zero components of the parity-check matrix are constructed with circulant matrices obtained by circular shifts of the unit matrix. Figure 2 shows the configuration of a decoding circuit for a QC-LDPC code If 1s are arranged at random in the parity-check matrix of an LDPC code, then anywhere from several thousand to several ten-thousand core modules for decoding operations (row operation cores, column operation cores) are arranged directly below the first level, and since each of these is irregularly connected, it becomes a hotbed for wiring congestion and timing violations. However, by adopting the configuration of a QC-LDPC code, it is possible to consolidate operation blocks in circulant matrix size units, and this enables circuit optimization and layout adjustment in block units. In QC-LDPC code design, the size of the circulant matrices and their shift amounts are also important parameters, and optimization is necessary to coordinate with the decoding circuit architecture and process rules.

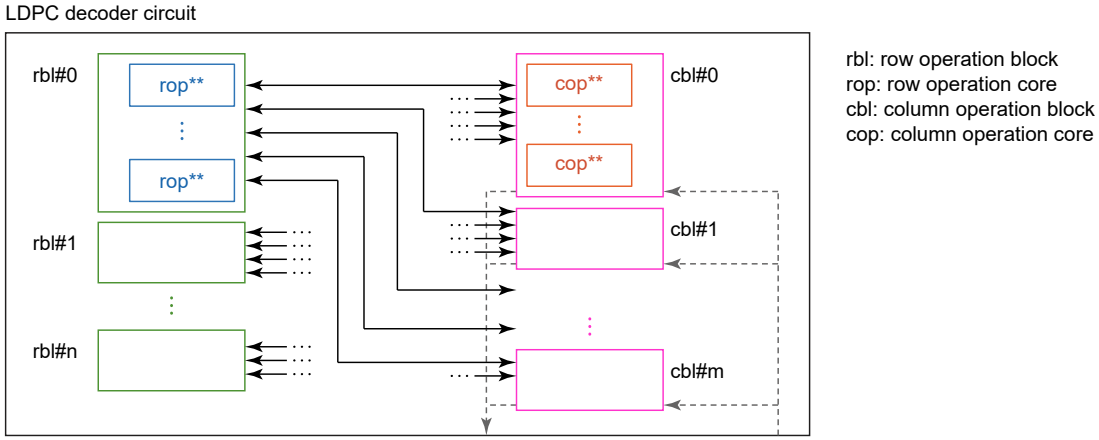

Fig. 2 QC-LDPC code decoder configuration example

3. Search for a QC-LDPC Code and Decoding Circuit Architecture Taking Circuit Characteristics into Account

Even if a QC-LDPC code is suitable for development as a circuit, the difficulty of layout design is still high, and trial-and-error is necessary to meet the required specifications. In the wafer manufacturing process in recent years, cell units have become smaller, and convergence of wiring onto those smaller cells has led to wiring congestion, and a greater tendency for timing violations to occur due to wiring delays for the purpose of avoiding congestion. The easiest way to resolve timing violations is to use high-speed cells provided for the purpose of increasing circuit speed, but these cells have the disadvantage of high power consumption. Also, cell characteristics fluctuate due to variability, voltage, temperature, and operating frequency, and conditions vary due to process rules, so the circuit architecture must be optimized to suit the applied process, code, and decoding algorithm[(2)]. Furthermore, the parity-check matrix has an effect not only on error-correction performance but also on circuit scale, and thus feedback design, where code design is based on decoding circuit physical synthesis results, is also necessary.

Table 1 shows trial results of design optimization for an error-correction circuit with 800Gbps throughput for an optical communication Application Specific Integrated Circuit (ASIC). With this design, the goal was to achieve the target performance from the standpoint of both code design and circuit design. With Method 1, goals were met for error-correction performance and power consumption, but timing violations and wiring congestion occurred, and the result had low feasibility. With Method 2, a pipeline approach was used

Table 1 Circuit design results for 800Gbps throughput forward error-correction decoder

Method	Overview of revision content	Code (Circulant matrix size)	Correction performance	Power Consumption (W) (800Gbps)	Soft-decision decoding circuit gate count (MG)	Error-correction circuit total gate count (MG)	Timing violation (ns)	Wiring congestion (%)	High-speed cell usage (%)
Target value	-	-	○	2.3W or less	11MG or less	-	-0.01	0.1% or less	10% or less
Method 1	400G per 1blk, 2-parallel configuration	Code A (96)	○	1.92	11.5	54.3	-0.19	39.00	32.36
Method 2	Pipeline decoding processing	Code A (96)	○	2.13	13.4	60.8	-0.54	1.24	29.69
Method 3	Lengthening short code of QC-LDPC code 100G per 1blk, 8-parallel configuration	Code B (64)	△	2.88	10.6	78.6	-0.40	0.10	37.72
Method 4	Reduction of decoding operation bit width of Method 3	Code B (64)	×	2.48	8.9	67.2	-0.27	0.15	30.94
Method 5	Lengthening short code of QC-LDPC code Higher performance of concatenated hard-decision code	Code C (64)	○	2.75	8.7	82.0	-0.11	0.12	22.08
Method 6	Application of 1/2 operating frequency 100G per 1blk, 8-parallel configuration	Code C (64)	○	2.30	10.9	105.2	0	0.09	0.27

to avoid wiring congestion, but the outlook for circuit feasibility was poor, and there was feedback on code design and decoding circuit architecture in terms of code length and circulant matrix size. Finally, all goals were achieved with Method 6, in which optimization of operating frequency is added to the circuit architecture formulated in Method 3 and a redesigned code.

4. Dynamic Power Saving Method Using Decoding Circuit Control Considering Eevice Characteristics

The error-correction decoding circuit increases in scale in proportion to increasing transmission capacity, and there are limits on static power reduction through decoding processing simplification and circuit implementation technology alone. Thus low power must be achieved through dynamic circuit control that takes into account characteristics in terms of equipment operation.

By exploiting the high error-correction performance of QC-LDPC codes used for optical communication, it is possible to tolerate occurrence of errors in transmission paths, and this enables extension of transmission distances. However, when operation of optical communication equipment is considered, it is typical to operate in a range with a certain margin with respect to the error-correction limits. In other words, in actual operating ranges, received signals with higher signal quality than those near the error-correction limit can be obtained, so power consumption can be reduced by monitoring the signal degradation state on a code-by-code basis and dynamically stopping the decoding circuit to avoid unnecessary calculations[3]. Figure 3 shows the power reduction effect due to decoding operation control based on signal quality. The horizontal axis indicates the offset SNR (Signal to Noise Ratio), taking the error-correction limits as a basis, and the vertical axis shows normalized power consumption, taking as a basis the power when there is no dynamic stopping of decoding circuits. At the error-correction limits, or on transmission paths with characteristics worse than that (negative side), the error-correction decoding circuits operate constantly, and power consumption approaches 100%. By operating, in contrast, in a range with a margin of at least 0.5dB with respect to error-correction limits, results have been obtained where power consumption can be reduced close to 40% from that at maximum operation.

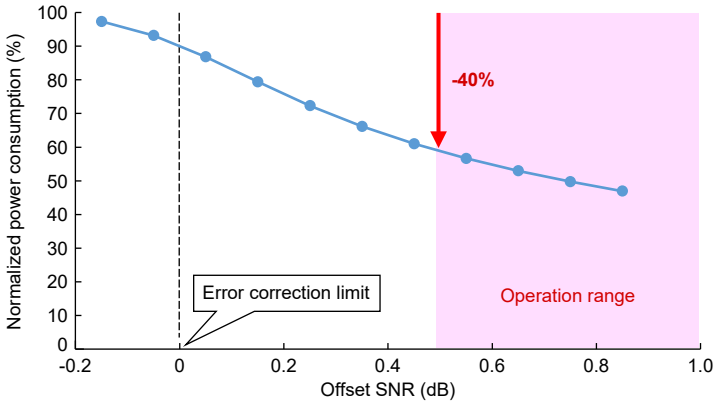

Fig. 3 Power reduction effect by decoding operation control according to signal quality

5. Conclusion

Using the LDPC code for 800Gbps high-capacity optical communications as an example, we described low-power design technology for error-correction circuits using advanced wafer manufacturing processes. As communication networks become larger in capacity, there is a demand for the contradictory characteristics of improved correction performance and low power consumption at the same time. However, the demand for low power consumption can no longer be met by advances in wafer manufacturing processes alone. To achieve these goals, dynamic power saving that takes advantage of the operational characteristics of the equipment described in this paper is likely to become increasingly important.

In addition, while this paper uses the ASIC development of an error-correction circuit for optical communications using advanced wafer manufacturing processes as an example, the same is also valid for FPGA (Field Programmable Gate Array), which is becoming increasingly miniaturized. In FPGA, the circuit resources available for each device are limited, so digital design technology that integrates system/application characteristics with implementation characteristics is important, along with optimization from both the code design and circuit design perspectives.

References

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