Development of SiC Trench MOSFET with Novel Structure Enabling Lower Losses

Authors: *Katsutoshi Sugawara** and *Yutaka Fukui* **

1. Introduction

Amid growing environmental awareness, the energy efficiency of power electronics equipment has been improved and SiC has been attracting attention as the next-generation power semiconductor material. Compared to conventional Si, the band gap of SiC is wider and the breakdown field is higher; moreover, SiC power devices have excellent properties. Mitsubishi Electric Corporation has been developing and mass-producing SiC-MOSFETs and SiC-SBDs and has commercialized products with a wide range of breakdown voltage classes, from 600 V for home appliances to 3.3 kV for electric railways.

To improve the energy efficiency of power electronics equipment, it is important to reduce the loss of the power devices used for such equipment. Mitsubishi Electric has been using planar-gate MOSFETs which feature low resistance. Meanwhile, for trench-gate MOSFETs, which have a structure where gate electrodes are vuried in the drift layers, the unit cell size can be reduced compared to the planar type while higher integration is expected to reduce the on resistance. However, electric fields tend to concentrate on the trench bottoms of the trench type and such electric fields need to be reduced to ensure device reliability. Previously, Mitsubishi Electric proposed a structure where a p-type protective layer (BPW) provided at the trench bottom was grounded to reduce the electric field.[1] However, as shown in Fig. 1(a), higher integration was difficult because the unit cell pitch depends on the size of BPW contact cell. To solve this problem, we developed the MIT2-MOS with a new device structure featuring an improved contact structure.

This paper describes the structure and performance of the MIT2-MOS.

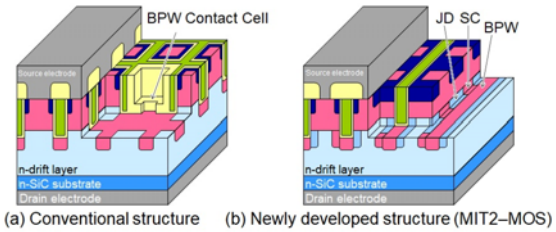

Fig. 1 Schematic diagrams of trench-gate MOSFET

2. MIT2-MOS

2.1 Structure of the MIT2-MOS

The MIT2-MOS is characterized by three implanted layers. Figure 1(b) is a schematic diagram of the MIT2-MOS.

The first layer is a BPW at the trench bottom and this is formed by opening a trench on the SiC drift layer and implanting p-type ions from the directly facing position. This BPW alleviates a high electric field applied to the trench bottom as described in Section 1. However, the potential of floating BPW is unstable, it causes the switching loss increases. In addition, a depletion layer formed by the BPW causes narrowing of the current paths between the PW and BPW and between the BPW and BPW, increasing the resistance.

The second layer SC is provided to solve the former problem. This is formed by implanting p-type ions diagonally to the opened trench. The BPW is grounded by the SC, which stabilizes the BPW potential and reduces the switching loss.[2]

The third layer JD is provided to solve the latter problem. It is formed by implanting n-type ions diagonally to the trench. Providing an n-layer with higher ion density than the n-SiC drift layer suppresses expansion of the depletion layer from the BPW and prevents the resistance from increasing due to narrowing of the current paths.[3]

MIT2-MOSs can be manufactured by low-energy ion plantation by tilted ion implantation to the trench walls. In addition, epitaxial re-growth after ion implantation is not required and so the devices can be manufactured by simple processes. Another advantage is that higher integration is easier thanks to the simple structure.

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2.2 Static characteristics of the MIT2-MOS

Generally, a MOSFET's threshold voltage (Vth) is in a trade-off relationship with the specific on resistance (Ron). Decreasing Vth lowers the Ron. However, a lower Vth makes it easier for a leakage current between the drain and source. In addition, Vth decreases as the temperature increases and so a high Vth is required depending on the application. Figure 2 shows the relationship between Ron and Vth. The assumed voltage class is 1.2 kV and the actual avalanche voltage is 1.5 kV. The graphs show that the increase in Ron in the high Vth region is suppressed for the trench type compared to the conventional planar type. For example, when Vth is 4.1 V, Ron is 1.9 mΩcm^2. This value is approximately half that of the planar type. Although Mitsubishi Electric reported that an increase in Ron could be suppressed in the high Vth region even for the planar type by applying re-oxidation to gate process,[4] the trench type offers superior improvement effect.

Meanwhile, the input capacitance Ciss of the trench type is larger than that of the planar type because of an increase in the channel width density. As a performance index of FOM (figure of merit) for this, the product (RonCiss) of specific on resistance and input capacitance in Fig. 3 is often used. This index for the trench type is slightly smaller than that for the planar type and the trench type's product (RonCrss) of the specific on resistance and reverse capacitance is almost the same as that of the planar type. These results show that for chips with the same Ron, the chip size of the trench type is smaller and its Ciss is also smaller.

2.3 Dynamic characteristics of the MIT2-MOS

Table 1 compares the dynamic characteristics. When comparing the planar-gate MOS and MIT2-MOS at the same dV/dt by adjusting the external gate resistance Rg, dI/dt of the trench type is larger than that of the planar type. Although this makes the turn-on loss (Eon) smaller, the turn-off loss (Eoff) of the trench type is larger. When the external gate resistance of the turn-off is changed such that dV/dt becomes equal to that of the turn-on and dV/dt and dI/dt are made larger, the sum of the trench type's Eon and Eoff is smaller than that of the planar type.

2.4 Reliability of the MIT2-MOS

As described in Section 1, the electric field at the trench bottom of the trench type tends to be larger than that of the planar type. In addition, the crystalline face on which a gate oxide forms differs between the trench type and planar type and it is known that when strong gate stress is applied to the trench type, Vth shifts.[5] Gate stress was applied to the MIT2-MOS and changes in the properties were examined. Figure 4 shows the results. When Vth was increased by 0.23 V by applying stress, the increase in Ron was approximately 2% at room temperature and only 1% or less at 150°C. This is equal to the increase in Ron when Vth increased by 0.23 V in the relationship between Ron and Vth shown in Fig. 2. This reveals that the increase in Ron is caused only by the increase in Vth and that Ron itself is not increased by the application of stress. The switching loss also shifts in line with the increase in Vth and the sum of Eon and Eoff before the stress was applied is the same as that after the stress was applied.

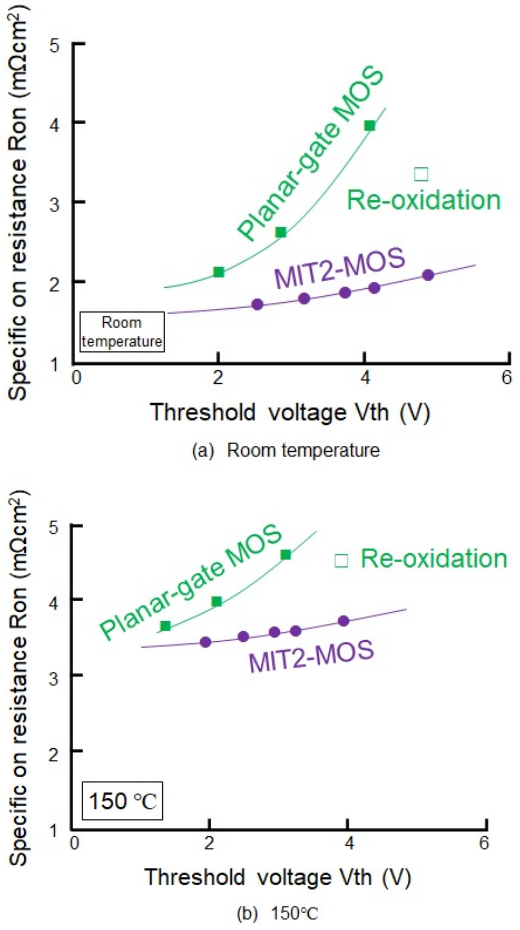

Fig. 2 Relationships between Ron and Vth for planer-gate MOSFET and MIT2-MOS at (a) R.T. and (b) 150 ℃.

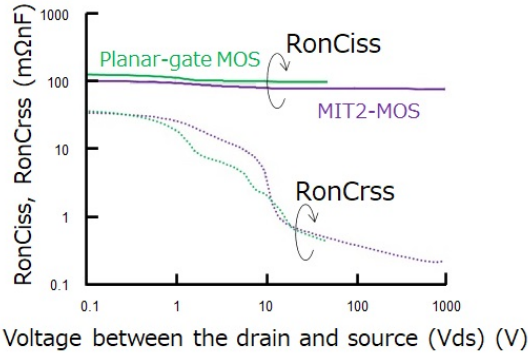

Fig. 3 Vds dependences of RonCiss and RonCrss

Vth shift may be caused by changes in the state of the gate oxide. To confirm this, two devices after stress was applied were subjected to a high-temperature reverse bias (HTRB) test. Figure 5 shows the changes in Vth measured during the test. As the stress was applied for a longer time, Vth decreased and after 200 hours, Vth hardly changed. The Vth shift amount when the application of stress began was 0.23 V, and had reduced by 0.20 V after 200 hours had passed, but then changed little up to 1,000 hours. These results show that 0.20 V among the shift amount of 0.23 V is a temporary shift and it changes based on the stress applied to the device. In addition, as a result of a 1,000-hour HTRB test, the increase in Ron and leakage current is limited to 5% or less. These results show that even devices for which Vth shift has occurred are not degraded by a HTRB test.

Table 1 Comparison of SW characteristics in planar-gate MOS and MIT2-MOS

		Planar-gate MOS	MIT2–MOS		
Threshold voltage Vth	V	1.8	3.7		
Turn-On					
Rg*1			A	B	A
dV/dt	kV/μs	8.0	8.0	6.0	8.0
dI/dt	kA/μs	1.8	2.1	1.78	2.1
Eon	mJ/P	1.1	0.8	1.8	0.8
Turn-Off					
Rg			B	B	A
dV/dt	kV/μs	10.0	10.0	10.0	15.0
dI/dt	kA/μs	0.9	1.1	1.1	2.6
Eoff	mJ/P	2.1	2.7	2.7	2.0
Eon + Eoff	mJ/P	3.2	3.5	4.5	2.8
vs planar type	%		+10.9	+40.6	-12.5

Note 1: Rg refers to the external gate resistance of the MOSFET.

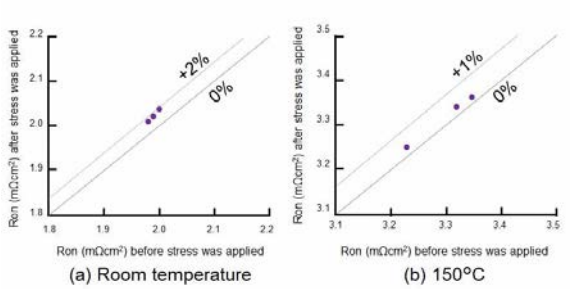

Fig. 4 Changes of Ron after gate stress at (a) R.T. and (b) 150 ℃.

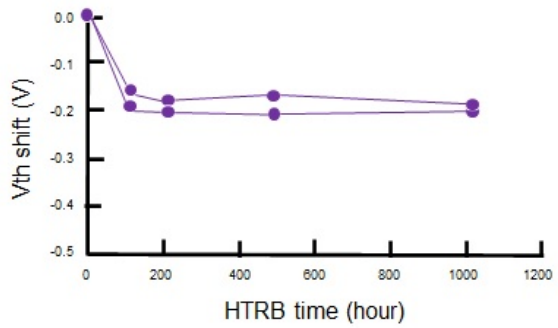

Fig. 5 HTRB stabilities of Vth after gate stress

3. Conclusion

We have developed MIT2-MOSs that include BPWs which alleviate the electric fields applied to trench bottoms, SCs that ground the BPWs, and JDs that prevent narrowing of current paths. The rating of the developed 1.2 kV class MIT2-MOS (avalanche voltage of 1.5 kV), the threshold voltage is 4.1 V, and the specific on resistance is 1.9 mΩcm^2. This latter value is approximately half that of the planar type which is being commercialized. In addition, a large stress was applied to the gate to cause Vth shift of 0.23 V and the influence on the static characteristics, dynamic characteristics, and HTRB reliability was examined. The results showed no significant problems. Furthermore, 0.20 V among the Vth shift of 0.23 V was found to be a temporary shift. Thus, we have confirmed that the developed MIT2-MOS has excellent performance. We will continue to work toward mass-producing it.

References

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