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CONTENTS

Technical Reports

Precis

The era of fifth generation mobile communication, automatic driving and IoT (Internet of Things) is fast approaching. The progress creates new demand and contributes to society by solving the problems of labor shortage, productivity improvement and so forth. This article introduces microwave and optical devices and the related technologies developed by Mitsubishi Electric Corporation that support the future progress.

Overview

Author: *Masayoshi Takemi**

The Status and Future Outlook of High-frequency & Optical Devices

Mobile communication devices such as smartphones and tablet terminals have become popular and their functions have been improved with each generation. Therefore, the total amount of mobile communication data in the world has been continuously increasing, further boosted by the age of vehicle automatic driving systems and the Internet of Things (IoT). New businesses are emerging with the growth of automatic driving and IoT, fueling new demand. These factors help improve productivity and solve the problems of the declining population and rising production costs, assuring the continued growth of society. Mobile communication systems support these developments, and fifth-generation (5G) mobile communication standards have now been developed. Furthermore, wireless communication at high frequencies (3.5 GHz to millimeter wave band) to achieve high speeds and large communication capacities is progressing. In this frequency band, gallium nitride (GaN) devices which can control power consumption efficiently are being developed at a fast pace.

In optical communication networks which are a core part of the communication infrastructure, systems with even higher speed and larger capacity are rapidly being developed. In the networks used for data centers, devices supporting 100 Gbps have been actively introduced and work on introducing 400 Gbps is progressing. As a result, for the optical devices mounted on these units, there is strong demand for compact size and reasonable cost in addition to high speed, low power consumption and high reliability. Research and development is underway to meet such requirements.

New applications of high-frequency devices and optical devices using compound semiconductors in diverse fields such as for projector light sources, lights including vehicle headlights, sensors, laser processing machines, and power supply devices have emerged in addition to the communications field. Thus, high-frequency devices and optical devices will serve as key components for the continued growth of society.

**Senior General Manager, High Frequency & Optical Device Works*

25-Gbps Can-type EML for 5G Mobile Base Stations

Authors: *Yojiro Watanabe** and *Yusuke Azuma**

To meet the demand for rapidly increasing communication data volumes, the fifth-generation mobile communication system (5G) is planned to be introduced from 2020. Large-capacity optical communication systems will be used at mobile base stations, and so an electro-absorption modulated laser diode (EML) which operates at 25 Gbps is required for the fronthaul optical module. In the present work, the transmission speed of 25 Gbps, the first in the industry, was achieved by a can-type EML.

1. Introduction

With the shift to 5G, the optical module used for each layer of the mobile base station network must also be high speed. The distributed feedback laser diode (DFB), which operates at 10 Gbps, has traditionally been used for the fronthaul for 4G. However, for 5G, EML operating at 25 Gbps is required. The system is configured to transmit and receive the optical signal with one optical fiber, for which two types of EML with the wavelengths of 1,270 nm and 1,310 nm are required. In addition, regarding the configuration of the EML package, the can-type package which facilitates assembly for the bi-directional (BIDI) module is required.

Popular EML products which operate at 25 Gbps use the box-type package (Fig. 1 (a)) which integrates ceramics and metal. However, with the can-type package (Fig. 1 (b)), band limitation due to impedance mismatch occurs, and it is difficult to obtain a satisfactory band for operation at 25 Gbps [1].

(a) 25-Gbps box-type EML (b) 25-Gbps box-type EML

Fig. 1 25-Gbps Box- and can-type EML

In this study, to increase the band of the can-type package, the 3-dB bandwidth of the frequency response characteristics was improved by controlling multiple reflection arising from impedance mismatch in the package. The EML device is designed to achieve both high output and high speed, and an extinction ratio of 6 dB or more and good optical output waveform were obtained. In addition, the low power consumption of the conventional box-type was achieved by using a compact Peltier cooler and by reducing heat flow to the EML under temperature control. In this way, operation at I-temp (−40 to 95°C) was achieved.

2. Package Outline

The outline dimension of the can-type package is Φ5.6 mm which is the industry standard, and each pin layout is compatible with our 10-Gbps conventional products. Since the EML has large characteristic fluctuation due to temperature variation, it is necessary to control the EML temperature to a constant level using a Peltier cooler and thermistor. To control the current in the laser diode of the EML to a constant level, a photo diode which monitors the backlight output is also built into the unit. The lens cap is a general cylindrical shape and is designed to facilitate the BIDI module, using welding technology.

3. Design Result of EML Device

The waveguide at the laser diode of the EML is designed to be an embedded type which is excellent in efficiency and high-temperature operation. The electro-absorption (EA) modulation unit is designed to have a large length and narrow width so that both low modulation voltage and high-speed operation can be satisfied. The high-mesa waveguide, which can maintain a high optical confinement factor in a narrow width design, is used [2]. As described above, the different waveguide designs between the laser diode and the EA modulation unit provide excellent characteristics of both designs. In addition, a spot-size converter at the end of the device widens the spot size of the beam emitted from the EML and improves the coupling efficiency with an optical fiber through the lens.

4. Design Result of Can-type Package

The band degradation of the can-type package is attributed to impedance mismatch between the driver IC operating the EML and the EML device mounted on the package. In particular, since band degradation tends to occur due to electric multiple reflection generated between the glass penetration area of the package lead and the EML device, the bandwidth was improved by

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reducing the impedance mismatch including the transmission channel inside the can-type package. If 50Ω match is configured inside the can-type package, the 3-dB bandwidth of the frequency response characteristic stays at 14 GHz. In contrast, the 3-dB bandwidth was improved to 19 GHz by controlling multiple reflection after improving the impedance matching.

5. Evaluation Results

Table 1 shows the product specifications and evaluation results of the 25-Gbps can-type EML. Figure 2 shows the evaluation results of the frequency response characteristics. The 3-dB bandwidth of the pass characteristic was 19.2 GHz. Figure 3 shows the back-to-back optical output waveform with the wavelength of 1,270 nm. The operating conditions were: bit rate 25.8 Gbps, case temperature (T_c) 25°C, EML setting temperature (T_{ld}) 55°C, LD operation current (I_{op}) 100 mA, modulation voltage swing of EA (V_{pp}) 2 V, and bias voltage of EA (V_{off}) −1.3 V. For the evaluation, a flexible printed circuit was connected to the can-type package. After evaluating the can-type EML with the wavelength of 1,270 nm, a good optical waveform with the extinction ratio of 6.8 dB, mask margin @ CWDM4 of 37% and jitter (RMS) of 1.5 ps was obtained. The evaluation results of the can-type EML with the wavelength of 1,310 nm are shown in Table 1.

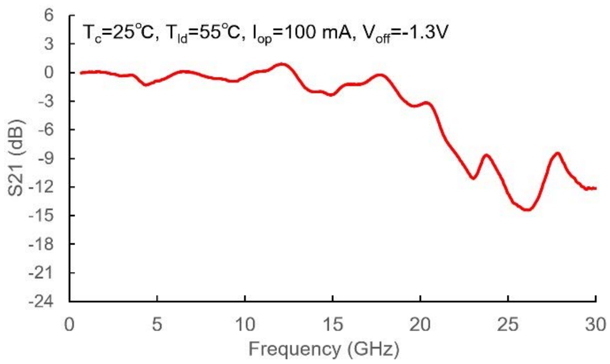

Fig. 2 Experimental results of frequency response

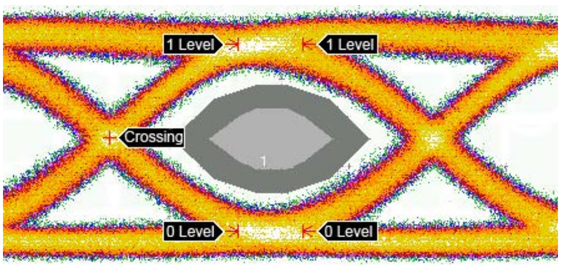

Fig. 3 25.8-Gbps eye diagram at 1,270 nm

Extinction ratio: 6.8 dB, Mask margin: 37%, Jitter (RMS): 1.5 ps

Figure 4 shows the power consumption of the Peltier cooler when the case temperature was changed from −40°C to 95°C. For comparison, the power consumption of the box-type package product mounted with the same EML device is also shown. Tld is 55°C and Iop is 100 mA. The power consumption of the Peltier cooler at the case temperature of 95°C was 0.32 W and the power consumption at −40°C was 0.52 W. This shows that both power consumptions decreased by about 30 to 40% in comparison with the box-type package products, indicating the effect of reducing the thermal input to the Peltier cooler.

6. Conclusion

We developed a 25-Gbps EML mounted on a can-type package for 5G. By improving the impedance matching inside the can-type package, the bandwidth was widened, and 19.2 GHz was achieved in the 3-dB bandwidth. The optical waveform of this newly-developed product was evaluated. With both the can-type EML having the wavelength of 1,270 nm and

Table 1 Specifications and experimental results of 25-Gbps can-type EML

Item	Product specification	Evaluation result
Emission wavelength	1,270 ± 10 nm 1,310 ± 10 nm	1,274 nm 1,309 nm
Optical output (CW) @ Iop = 100 mA	≥ 10 dBm	12.4 dBm
3 dB cutoff frequency	–	19.2 GHz
Extinction ratio	≥ 5 dB	6.8 dB @ 1,270 nm 7.8 dB @ 1,310 nm
Mask margin @ CWDM4	–	37% @ 1,270 nm 29% @ 1,310 nm
Jitter (RMS)	–	1.5 ps @ 1,270 nm 1.5 ps @ 1,310 nm
Power consumption of Peltier cooler	≤ 0.7 W @ −40°C ≤ 0.42 W @ 95°C	0.52 W @ −40°C 0.32 W @ 95°C

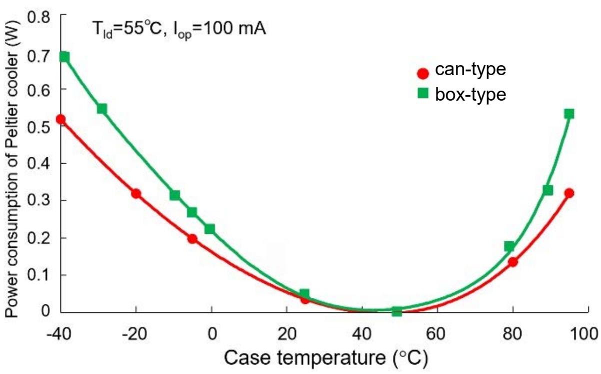

Fig. 4 Experimental results of power consumption of Peltier cooler

1,310 nm, the back-to-back values were: extinction ratio was 6 dB or more, mask margin @ CWDM4 was 29% or more and jitter (RMS) was 1.5 ps. In addition, the compact Peltier cooler and reduced thermal input lowered the power consumption by about 30 to 40% compared to conventional products. The power consumption of the Peltier cooler at the case temperature of +95°C is 0.32 W, which allows for operation at I-temp (−40 to +95°C).

7. References

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400-Gbps Compact Integrated EML-TOSA

Author: *Yudai Imai**

1. Introduction

To meet the rapid increase in traffic along with higher speed and larger capacity of optical transmission devices, a transceiver that can handle larger-capacity communication is required by changing the conventional optical transceiver with transmission capacity of 100 Gbps (1). To meet such requirements, two TOSA, one with a short-wavelength bandwidth and the other with a long-wavelength bandwidth, were combined (8 wavelengths) based on the 100-Gbps small integrated EML-TOSA. A product conforming to a transceiver with a transmission capacity of 400 Gbps was thus developed for operation in the newly employed PAM-4 modulation system.

2. Device Specifications

The newly developed 400-Gbps small integrated EML-TOSA meets the specifications of 400GBASE-LR8 which is 8 wavelengths and a transmission distance of 10 km standardized by IEEE. The TOSA size conforms to CFP8 which is the package standard of the 400-Gbps optical transceiver. The operating temperature range is −5°C to 80°C for the temperature of the case. If operated in the PAM-4 modulation system, it can operate at a maximum bit rate of 53.125 Gbps.

3. Device Design

Figure 1 shows a photo of the appearance. The package integrates both metal and ceramics. For the interface of electric signals, two FPC for the RF connection which sends modulating signals and for the DC connection which supplies power to LD, PD and TEC were used for connection. The FPC was directly connected to the metal pattern with narrow spacing on the ceramic to make the package small. The FPC for RF connection used a three-layer structure. The layout of the signal wire in the internal layer of the FPC widened the space between electrodes at the connection, and by maintaining the electrode distance to avoid shorting, ideal impedance matching was achieved (2).

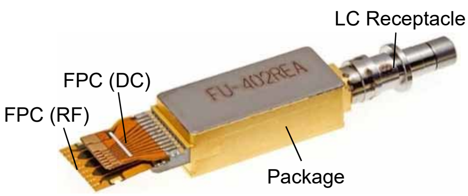

Fig. 1 400-Gbps compact integrated EML-TOSA

The size of the package area for one unit is 15.0 × 6.5 × 5.4 mm, which allows two units to be mounted on the CFP8 transceiver (3).

4. Optical System and Mechanism Design

Figure 2 shows a conceptual diagram of the optical system inside the TOSA. Inside the package, four EMLs, a lens and a spatial optical multiplexer are integrated. The optical multiplexer consists of three BPFs and one mirror, and they are fixed to a block member. This product uses the two-lens optical system. The first lens is mounted inside the package and the second lens is mounted outside the package. The collimated light through the first lens enters the spatial optical multiplexer and four wavelengths of lanes 0, 1, 2 and 3 are combined by multiple reflection between the BPFs and the mirror (4).

The difference between the two TOSAs (one for short wavelength and one for long wavelength) is the wavelength only. Since the internal structure is identical, they can be assembled in the same process.

5. PAM-4 (Pulse Amplitude Modulation 4)

Figure 3 shows the outline diagram of the optical waveform in PAM-4 modulation. This modulation system

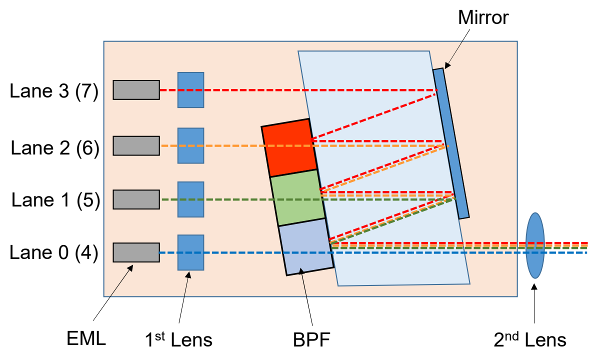

Fig. 2 Conceptual diagram of optical system

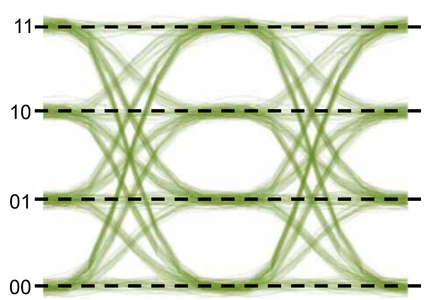

Fig. 3 Eye diagram by PAM-4 (Simulation)

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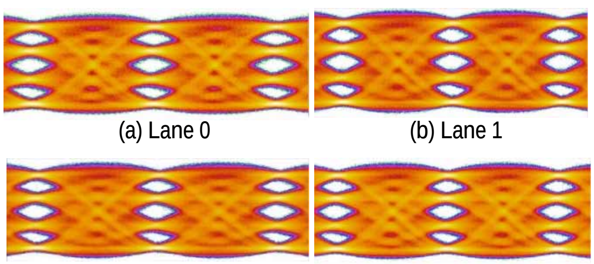
(4-level modulation) modulates and transmits the bit row consisting of "0" and "1" as the pulse signal of four voltage levels of "00," "01," "10" and "11." The transmission capacity per hour is twice that of the NRZ modulation system which uses 2-level.

For the PAM-4 modulation system, TDECQ is a particularly important evaluation parameter which shows the degree of three eye openings equivalent to the eye mask test of NRZ. The signal error rate is obtained from two elements of the signal distribution: the specified UI and the optical output threshold, and TDECQ is the value obtained from the signal error rate. Although the definition is different, TDECQ means evaluation of the error rate and communication quality, similarly to the eye mask test for the NRZ modulation waveform. The standard for this TDECQ specifies 3.3 dB or less in the Institute of Electrical and Electronics Engineers (IEEE) which performs standardization activities [5].

6. Evaluation Results

Figure 4 shows the measured optical waveform (shortwave length side). EML modulates all lanes in PAM-4 simultaneously. All lanes obtained good eye-opening characteristics with the extinction ratio of 8 dB or more and TDECQ of 2.7 dB or less under the conditions of the EA modulator voltage amplitude of 1.40 V.

Figure 5 shows the relationship between the total TEC power consumption of two TOSAs and the case temperature when the chip drive temperature is set to 60°C.



(a) Lane 0 (b) Lane 1

(c) Lane 2 (d) Lane 3

Fig. 4 Eye diagram by PAM-4 (Measurement)

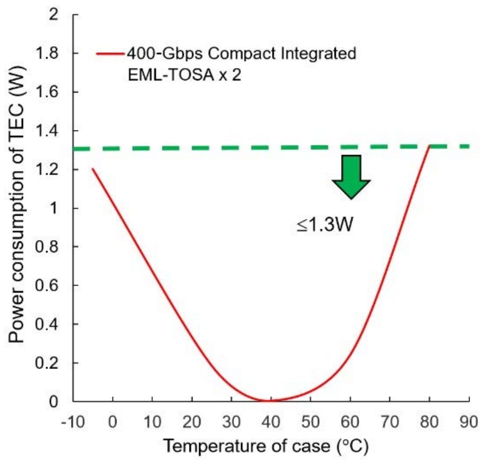


Fig. 5 Power consumption of TEC (LD current: 100 mA)

The TEC power consumption for one TOSA is equivalent to the 100-Gbps small integrated EML-TOSA. The TEC power consumption is controlled to 1.3 W or less for two units in the operating temperature range from −5 to 80°C. This system supports higher transmission capacity and yet suppresses an increase of power consumption.

7. Conclusion

We have developed a small integrated EML-TOSA which supports large-capacity high-speed transmission of 400 Gbps with two TOSAs, which can be mounted on CFP8.

This product will contribute to the spread of optical transceivers in 400-Gbps networks, a market which is expected to expand rapidly in the future. We will leverage the knowledge gained with this product and the PAM-4 modulation system to develop a smaller TOSA which can be mounted on the QSFP-DD platform, enabling the transceiver to be made more compact.

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High-Power 638-nm Red Laser Diode with Built-in Lens for Display Applications

Authors: *Fumio Shohda** and *Kohei Sakai**

A red semiconductor laser diode (LD) with small built-in lens was developed by applying the principle of the optical beam expander in the slow axis (horizontal) direction where three emitters (emitting point) are lined up. In this product, a pulsed 2.5W collimating beam with divergence angle of 3.6°×0.5° (typical value) was realized.

1. Background

In contrast to the high-pressure mercury lamp which is widely used as a light source for projectors, a semiconductor laser with good color reproduction, high efficiency, low power consumption and high brightness is attracting attention. We have developed a high output red semiconductor laser, ML562G84, with a pulse light output of 2.5 W, for display application.

In this product, the output laser light has a large divergence angle. To radiate the laser light on the display efficiently, an external collimating lens is required. However, since the design has a large divergence angle in the fast axis (vertical) direction and three emitters in one LD chip, the optical design is difficult and the application range is limited.

Therefore, we developed the lens by applying the principle of the optical beam expander in the slow axis direction where three emitters are lined up. This paper describes the design of the collimating lens and various characteristics of the product.

2. Design Review of Lens for Red Pulse LD

Our red pulse LD uses an AlGaInP based material mounted on the TO-CAN package of 9.0 mm diameter. After studying the optical output characteristics and reliability, a multi-emitter design having three emitters consisting of a broad stripe LD of 60 μm width was selected. The divergence angle full widths (FW1/e^2M), which make the optical output 1/e^2 of the peak value in the far field, are 8.0° and 69.0° (typical values), respectively. In particular, the divergence angle of the vertical direction is relatively larger.

When designing a collimating lens which is suitable for these LD device designs and far-field characteristics, the following problems are encountered. First, the width of three emitters in the LD horizontal direction is 270 μm, which is rather wide. To make the divergence angle small, it is necessary to increase the focal length of the lens, but this makes it necessary to increase the effective opening of the lens to improve the light use efficiency because the divergence angle in the LD vertical direction is large. Thus, in a general axisymmetric lens, the desired lens performance has a trade-off relationship with a compact lens size.

Therefore, we designed a lens by applying the principle of the optical beam expander in the horizontal direction having three emitters lined up. The beam expander enlarges the beam diameter of the laser light and makes the divergence angle of the beam small. Figure 1 shows a schematic of the collimating functions for each direction.

The principle of the beam expander is as follows. When lenses with focal lengths of f_1 and f_2 are placed at the distance of d, the beam is enlarged with magnitude m (= $-f_2/f_1$) determined by the ratio of the focal lengths. The relationships between the incident beam (divergence angle θ_0, beam diameter ω_0) and the generated beam (convergence angle θ_1, beam diameter ω_1) and between distance d and focal lengths f_1 and f_2 are as follows:

$$\omega_1 = (-f_2/f_1)\,\omega_0 = m\omega_0 \tag{1}$$

$$\theta_1 = (-f_1/f_2)\,\theta_0 = \theta_0/m \tag{2}$$

$$d = f_1 + f_2 \tag{3}$$

The parameters of each lens were optimized by applying this principle to the horizontal direction and considering the limitations of lens manufacturing. On the other hand, in the vertical direction, we collimate at output surface by employing the conventional way. The lens position for the LD in the optical axis direction is the constant beam divergence angle in the horizontal direction, which is independent of the distance between the LD and the lens. Therefore, lenses were placed at the position of the focal length in the vertical direction. Figure 2 shows the calculated beam pattern at each

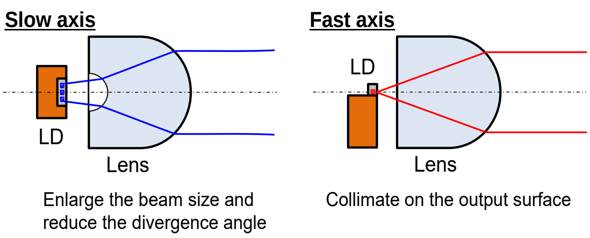

Fig. 1 Collimating functions for each axis

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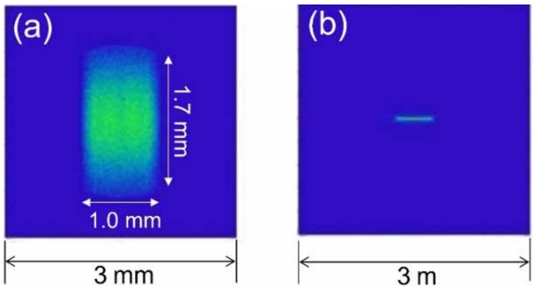
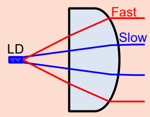
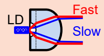


(a) Lens output surface (b) Far field pattern

Fig. 2 Calculated results of beam profile

Table 1 Comparison of lens configuration

Item	Conventional (Axisymmetric)	This work
Configuration		
Size	Large	Small
Divergence angle in slow axis	Equivalent	
Cost	Equivalent	

position after emission from the lens. The beam diameter immediately after the lens is 1.0 mm in the horizontal direction and 1.7 mm in the vertical direction. The divergence angle (FW1/e^{2}M) in the far field is 3.5° in the horizontal direction and 0.2° in the vertical direction.

Table 1 shows a comparison of the axisymmetric lens configuration and the developed lens configuration. In this development, the principle of the beam expander in the horizontal direction was used and a compact projector light source was achieved. With the optimum design and small lens diameter based on the lens manufacturing conditions, costs equivalent to those for normal lenses were achieved.

3. Laser Characteristics

Figure 3 shows the optical output vs. current characteristics of the developed product. The operating conditions are pulse operation with the duty ratio of 30% and pulse frequency of 120 Hz. The temperature in the figure is the temperature (case temperature) at the bottom of the package. The figure shows a photo of the appearance of the developed product. At 25°C and 2.5 W output, the operating current was 2.77 A, the operating voltage was 2.35 V and the slope efficiency was 1.17 W/A. The transmittance of the lens was 98% or more, and the pulse light output of 2.5 W was achieved with the operating current equivalent to that of the conventional pulse product. By using a large package with high heat dissipation, operation in the range from 0 to 45°C was confirmed. The peak wavelength was about 638 nm and the full width at half maximum of the spectrum was about 1.0 nm. Figure 4 is the far field

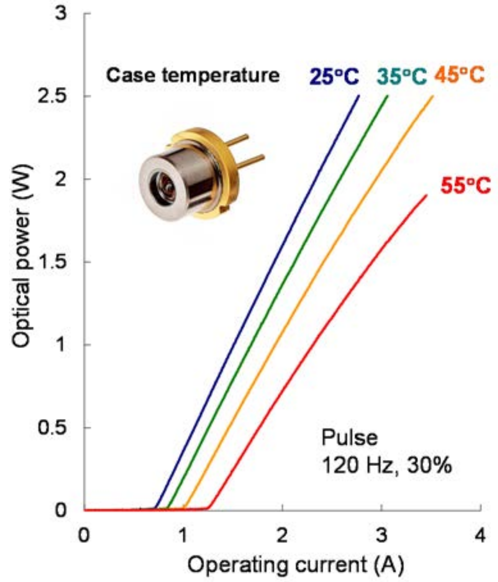


Fig. 3 P-I characteristics

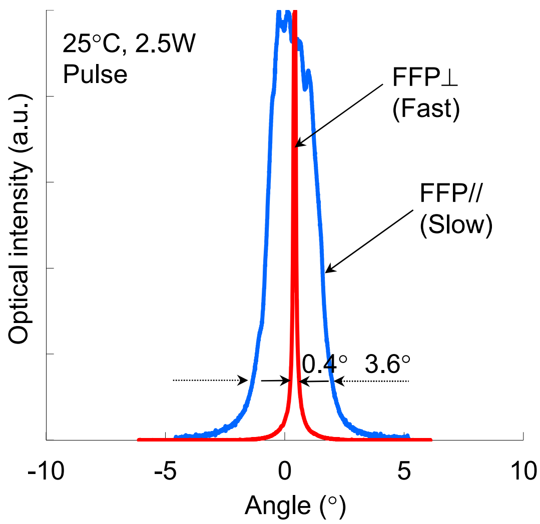


Fig. 4 FFP characteristics

pattern of the developed product in the horizontal direction (FFP//) and vertical direction (FFP⊥). The full width when the optical output is 1/e^2 of the peak value is 3.6° in the horizontal direction and 0.4° in the vertical direction. Considering the assembly tolerance of capping, a reasonable divergence angle was obtained as a result of the design.

4. Conclusion

In this study, we developed a high output red LD with lens which can be easily applied to projector systems. By applying the principle of the optical beam expander for the slow axis direction, a compact light source for projectors was achieved. As a result, parallel light of 3.6°×0.5° with a divergence angle full width (FW1/e^{2}M) which makes the light output 1/e^2 of the peak value was achieved.

This product can be used to simplify the optical design of projectors and to develop compact, low-cost optical devices. This red LD is expected to be increasingly used for projector light sources.

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Ultra-Wideband GaN Doherty Power Amplifier for Next-Generation Wireless Base Stations

Authors: *Yuji Komatsuzaki** and *Shuichi Sakata**

We have developed the ultra-wideband Doherty power amplifier to support the drastic increase in communication volume in next-generation mobile communication. The amplifier is able to handle multiple bands in mobile communication by combining the technology of absorbing the parasites of the transistor or package into the λ/4 inverter with circuit technology for compensating the frequency dependency, in addition to the GaN transistor which effectively widens the bandwidth.

1. Background

To meet the drastic increase in communication volume in next-generation mobile communication, the amplifier used for the mobile communication base station must be able to amplify signals with large peak to average power ratio (PAPR) with high efficiency and over a broad bandwidth. Broadband, which can support multiple bandwidths, is effective for reducing the size and cost of the base station. The Doherty power amplifier is a useful technology[1][2] which efficiently amplifies signals with large PAPR. However, one problem of the Doherty power amplifier is that it generally has narrow band characteristics in configuration.

This paper describes the gallium nitride (GaN) transistor, which is effective for the Doherty power amplifier for broadband applications. In addition, we report the development of an ultra-wideband Doherty power amplifier which covers multiple bandwidths used in 4G/long term evolution-advanced (LTE-advanced) by combining the technology of absorbing parasites of the transistor or package into the λ/4 inverter with circuit technology for compensating the frequency dependency.

2. Circuit Configuration of Ultra-Wideband Doherty Power Amplifier

Figure 1 shows the circuit configuration of the Doherty power amplifier. Figure 1 (a) shows the conventional circuit and Fig. 1 (b) shows the proposed circuit. In an ideal Doherty power amplifier, the configuration has two amplifiers in parallel and a λ/4 transmission line connected to the main amplifier. This λ/4 transmission line causes load modulation according to the operation of the two amplifiers, resulting in highly efficient operation at back-off. In contrast, in the conventional circuit of the practical Doherty power amplifier, the matching circuit and the offset line are connected to the output side of the main and auxiliary amplifier. In general, a transistor consisting of amplifiers requires a matching circuit which includes parasitic reactance and adjusts the output impedance to 50Ω. In addition, the offset line is required for adjusting electric length to occur resistive load modulation and is connected after the matching circuit. The λ/4 transmission line is connected to the main amplifier after the offset line. On the other hand, in the proposed circuit, the equivalent λ/4 transmission line including parasites of the package and the transistor is connected to the current source of the main amplifier transistor (Part A in Fig. 1 (b)) instead of the matching circuit and the offset line. In addition, the frequency dependency compensating circuit is connected to the output of the auxiliary amplifier (Part B of Fig. 1 (b)).

Figure 2 shows the circuit of the equivalent λ/4 transmission line (Part A in Fig. 1 (b)) including parasites

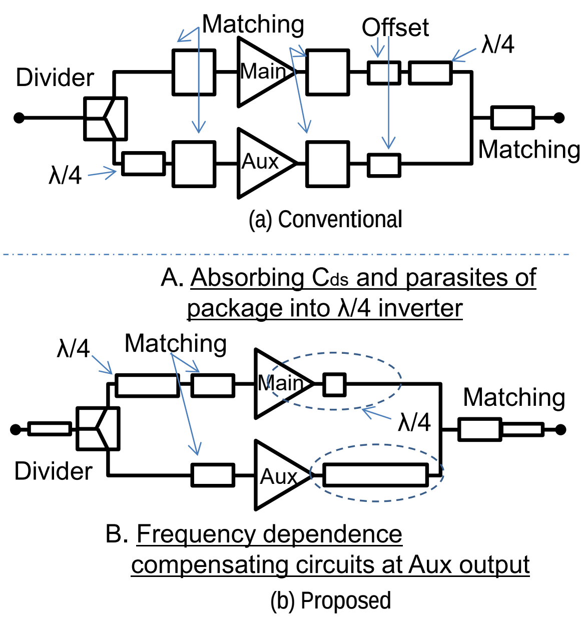

Fig. 1 Schematics of the Doherty power amplifier

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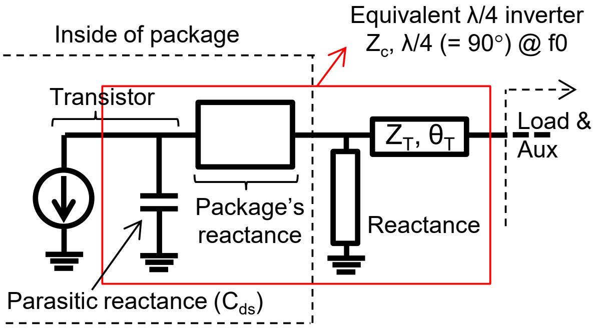

Fig. 2 **Schematic of the λ/4** inverter for absorbing the transistor output capacitance and reactance of package

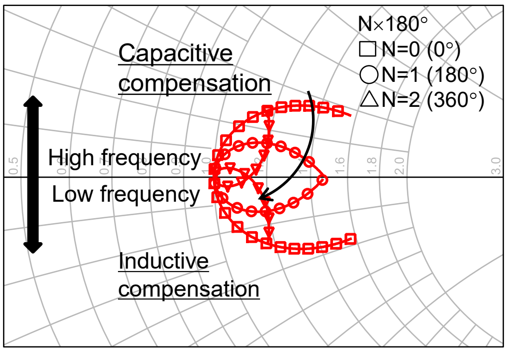

Fig. 3 Simulated frequency response of reflection at output terminal of the Doherty power amplifier

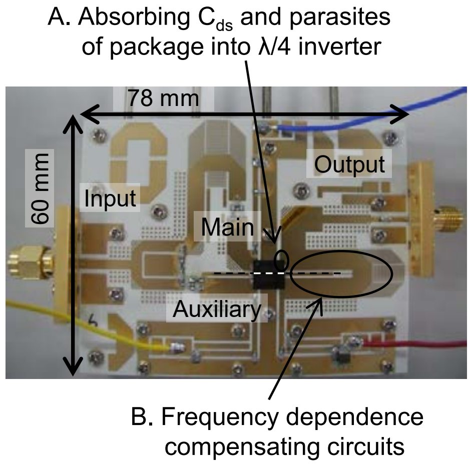

Fig. 4 Photo of the assembled ultra-wideband GaN Doherty power amplifier

of the package and the transistor. By combining parasites of the package and the transistor in Fig. 2 with the external circuit of the package, an equivalent λ/4 transmission line which has a characteristic impedance of Z_c and electric length of λ/4 at a certain frequency can be created. Since many Doherty power amplifiers include matching circuits and offset lines, the electric length from the current source of the transistor to the combining point of the main amplifier and auxiliary amplifier is larger than λ/4 wavelength or it has circuit elements for eliminating parasites. In contrast, our configuration directly connects the λ/4 transmission line to the current source of the transistor. The matching circuit or offset line is not connected as in the conventional circuit and the Doherty circuit can be configured with a broad bandwidth.

The frequency dependency compensating circuit (Part B in Fig. 1 (b)) compensates the frequency dependency of the λ/4 transmission line loaded on the main amplifier. This circuit is configured by including the package of the auxiliary amplifier and parasites of the transistor, and it has an electric length that is an integer (N) multiple of the λ/2 transmission line (λ/2) viewed from the current source of the auxiliary amplifier. The characteristic impedance and electric length are set to values so as to eliminate the frequency dependency of the λ/4 transmission line on the main amplifier. Figure 3 shows the simulation result of the frequency dependency of the reflection characteristic from the output terminal to the Doherty power amplifier. The electric length of the frequency dependency compensating circuit shows the simulation result of 0, λ/2×1 (180°) and λ/2×2 (360°). The frequency dependency compensating circuit is capacitive on the high-frequency side and inductive on the low-frequency side. This shows that impedance is concentrated on the real impedance axis. In the case of λ/2×2, the reflection coefficient is 0.14 or less over 20% of the fractional bandwidth and it is mostly matched with the broad bandwidth.

3. Measurement Result of Ultra-Wideband Doherty Power Amplifier

Figure 4 shows the manufactured ultra-wideband GaN Doherty power amplifier. Mitsubishi Electric's MGFS39G38L2 with two GaN high electron mobility transistors (HEMT) was used for the transistor of the Doherty power amplifier. In the Doherty power amplifier in Fig. 4, the upper path is the main amplifier and the lower path is the auxiliary amplifier.

Figure 5 shows the output power of the ultra-wideband Doherty power amplifier and the measurement results of the drain efficiency frequency characteristics. For the input signal, the LTE downlink signal with the bandwidth of 20 MHz and PAPR of 7.5 dB was used. Both the output power and efficiency in the figure are the maximum values, achieving ACLR = −50 dBc. In the broad bandwidth of 3.0–3.6 GHz, the drain efficiency of 45.9–50.2% is achieved, showing that this amplifier covers the multiple bandwidths of 4G/LTE-advanced.

4. Conclusion

We proposed a frequency dependency compensating circuit and ultra-wideband Doherty power amplifier incorporating parasites of the package and transistor into the output combiner. Prototype production

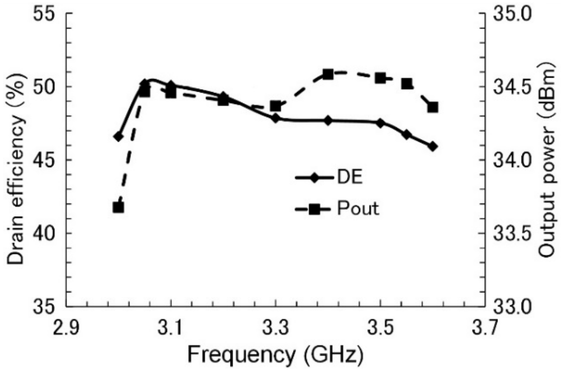

Fig. 5 Measured frequency dependencies of drain efficiency and output power

confirmed that this GaN Doherty power amplifier operates with a drain efficiency of 45.9–50.2% with the LTE signal in the 20 MHz bandwidth after satisfying −50 dBc by ACLR at the operating frequency range of 3.0–3.6 GHz.

This amplifier technology will enable the reduction of the number of transmitter amplifiers or power consumption, thus reducing the total cost of ownership of base stations.

5. References

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Thermal Analysis of GaN Device on Diamond Substrate with High Thermal Conductivity

Authors: *Koji Yoshitsugu** and *Eiji Yagyu**

This study investigated that the thermal resistance of a gallium nitride (GaN) device formed on a diamond substrate with high thermal conductivity. We experimentally confirmed that the thermal resistance of the GaN-on-diamond device was lowered by 45% and 70% compared with GaN-on-SiC and GaN-on-Si devices, respectively. By conducting steady-state thermal analysis considering the substrate thickness dependency, we found that only diamond was able to increase the reduction rate of the thermal resistance in case of thickening the substrate.

1. Introduction

As the detection distance of microwave radar has increased, the demand for high-output and highly efficient GaN high-frequency devices has grown. The main type of GaN high-frequency device used in industry is the GaN high electron mobility transistor formed on a semi-insulating silicon carbide substrate (GaN-on-SiC HEMT). However, its output density remains at about 10 W/mm owing to thermal limitations, and it is important to satisfy both high-reliability and high-output. To solve this problem, the concept of GaN-on-diamond thermal management design was recently proposed(1). Since the thermal conductivity of diamond is over 1,500 $Wm^{-1}K^{-1}$ at room temperature, which is the highest among solid materials, it may be useful for controlling local high-temperature areas (hot spots) during high-output operation (Fig. 1). Although it is quite difficult to manufacture the GaN-on-diamond HEMT, several papers have reported actual verification and that the output density was three times the conventional value(2). In this feasibility study, the thermal characteristics of a commercially-available GaN-on-diamond substrate were evaluated, focusing on the material properties.

2. Device Structures and Experimental Setup

As shown in Fig. 2, the device was formed by the same process for the AlGaN/GaN epitaxial layer on various substrates (Si, SiC and diamond). The substrate thickness of Si, SiC and diamond was 625 µm, 325 µm and 130 µm. To correspond to the spatial resolution of the thermal evaluation system, a Van-der-Pauw structure that is a relatively large active area of 0.4 mm^2 was employed. In addition, the chip area is much larger than the active area, so that the effect of the heat conduction can be evaluated. We measured the maximum temperature when energized with direct current using infrared (IR) thermography. The surface was coated with black paint to compensate for the emissivity of the material.

3. Thermal Resistance by Using IR Thermography

Figure 3 shows the temperature increase, ΔT of the device for dissipated power density. Thermal resistivity ρ_{th}. is determined from a linear slope of this graph. Thermal resistivity of the GaN-on-diamond device was 0.21 mm^2K/W. The reduction was 70% for GaN-on-Si

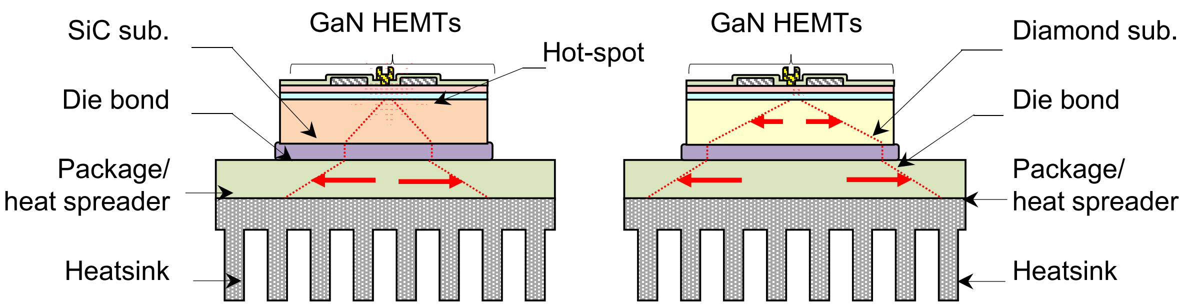

Fig. 1 Comparison of the effect of heat spread between conventional (GaN-on-SiC) and GaN-on-diamond device structure

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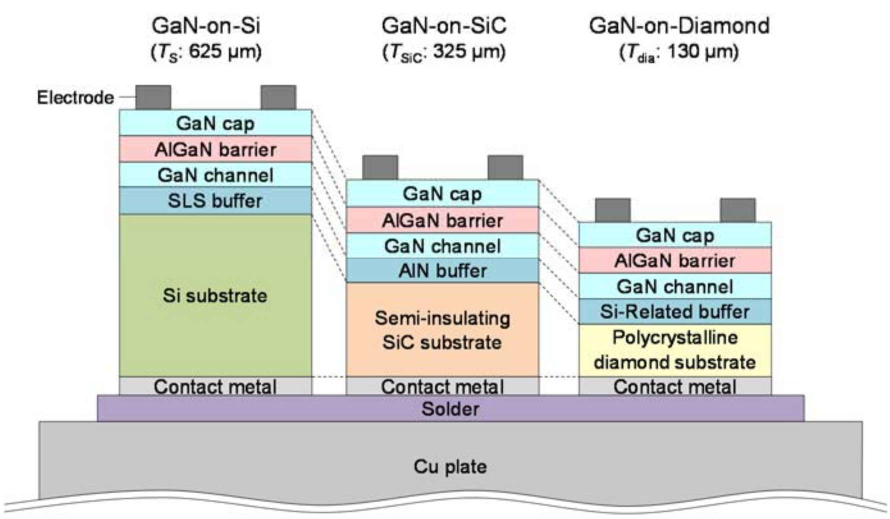

Fig. 2 Schematic cross section of fabricated GaN devices on various substrate for thermal evaluation

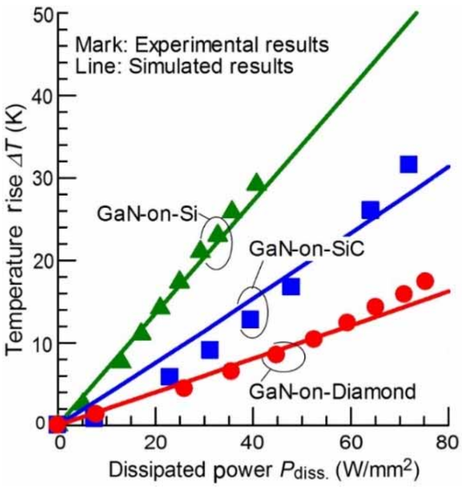

Fig. 3 Temperature rise versus dissipated power density

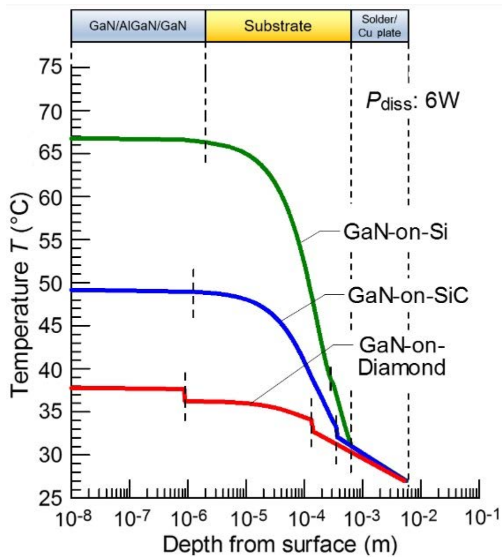

Fig. 4 Temperature distribution from the surface of the device in the depth direction at the dissipated power of 6 W

(0.71 mm^{2}K/W) and 45% for GaN-on-SiC (0.38 mm^{2}K/W). We demonstrated that the GaN-on-diamond has excellent thermal properties. However, it is noted that this result included the substrate thickness tolerance.

4. Thermal Analysis

Steady-state thermal analysis of the GaN-on-diamond structure was performed by using the numerical simulation for 3D finite element method. For the boundary conditions, the temperature at the back surface of the Cu plate was fixed and other outermost surfaces were vacuum-insulated.

Figure 4 shows the temperature distribution in the depth direction from the maximum thermal point at the dissipated power of 6 W. Figure 5 shows the thermal resistance of each layer structure calculated using the temperature difference. In the GaN-on-Si or the GaN-on-SiC, more than half of the total thermal resistance of the device is occupied by the thermal resistance of the substrate. In contrast, the substrate thermal resistance of GaN-on-diamond is limited to about 20% only, and the

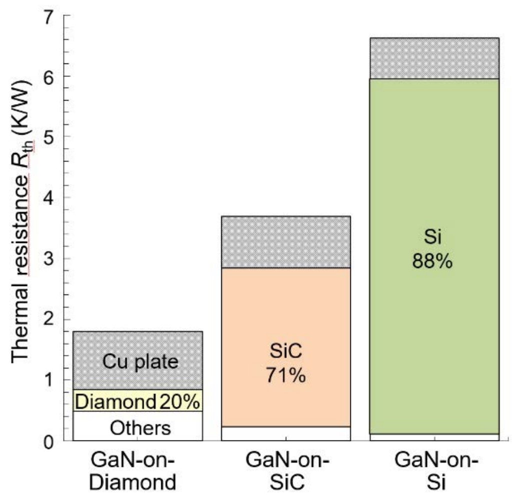

Fig. 5 Thermal resistivity and proportion of each layer structure of GaN devices

thermal resistance of the Cu plate is the largest. Thus, thermal analysis in the depth direction can be used to simply identify the rate-limiting factor of thermal resistance.

Since the substrate thickness of the GaN devices were not the same in this study, dependence of total thermal resistance on substrate thickness was calculated as depicted in Fig. 6.

It is expected that the thermal resistance is proportional to the heat transfer length, so that the total thermal resistance of the device for a thick substrate increase, regardless of the material. However, it actually increased for GaN-on-Si only; it stayed almost the same for GaN-on-SiC, and gradually reduced for GaN-on-diamond. Comparing the thermal resistance with a substrate of the same thickness for each, we found that the thermal management of GaN-on-diamond was more advantageous than the experiment result when the substrate thickness was 350 μm or more.

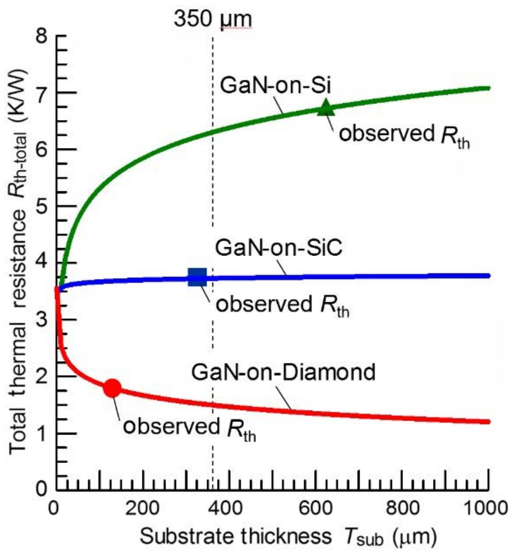

Fig. 6 Dependence of total thermal resistance on substrate thickness of GaN devices

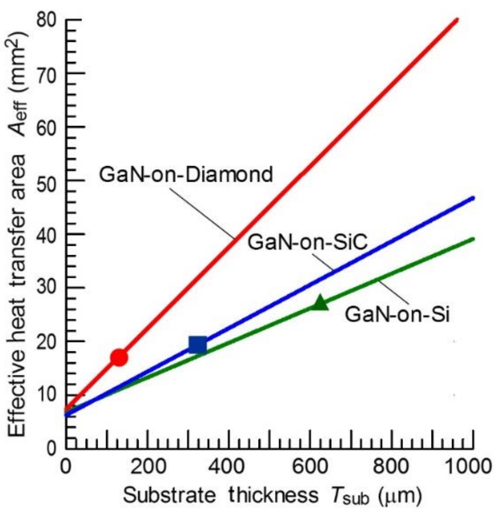

Fig. 7 Dependence of effective heat transfer area on substrate thickness of GaN devices

Figure 7 shows the effective heat transfer area $A_{eff.}$ determined from following equation [1], where L_i, k_i and R_{th_i} are heat transfer length, thermal conductivity and thermal resistance, respectively.

$$A_{eff.} = \sum_{i=1}^{n} A_i = \sum_{i=1}^{n} \frac{L_i}{k_i R_{th-i}} \qquad [1]$$

The effective heat transfer area, $A_{eff.}$ is defined as a total sum of a heat transfer area, A_i of each layer in the device. The difference of the rate of $A_{eff.}$ increase for the substrate thickness only corresponds to the difference in the substrate materials. The highest rate of $A_{eff.}$ increase in the GaN-on-diamond device suggests that a diamond has a superior heat spreading capacity. Therefore, we believe that the GaN device formed on thicker diamond exhibited thermal property advantageous. In addition, it is important to design a device geometry, chip area, and layer thickness for an optimum thermal management.

5. Conclusion

The thermal analysis of GaN-on-diamond substrate was performed by both experimental and simulation techniques. We confirmed that the GaN-on-diamond structure has more excellent thermal properties than GaN-on-Si or GaN-on-SiC which are the conventional substrate structures. Furthermore, we found that the total thermal resistance of the GaN-on-diamond decreased with increasing the substrate thickness due to the large effective heat transfer area. To optimize the thermal dissipation design, it is important to design the layer thickness, chip area and device layout according to the material type. This study may pave the way for the new development of GaN high-frequency devices.

6. Acknowledgement

This study was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

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Short-Gate Formation Process for High Throughput Production of GaAs-HEMT

Authors: *Takahiro Ueno** and *Kazuyuki Onoe**

As a substitute for fine resist pattern forming by electron beam (EB) lithography, we developed a method of forming fine resist patterns with high throughput, by combining i-line stepper exposure with the chemical shrink process. A resist trench of 0.39 μm was formed from the i-line stepper and the trench was reduced to 0.16 μm by the chemical shrink process. Using this process, we successfully formed a uniform L_g = 0.196 μm gate electrode.

1. Background

GaAs HEMT has excellent high-speed performance and low noise characteristics, and is widely used in micro- and milli-wave devices such as for satellite broadcasting, in-vehicle radar, etc. To improve the high-speed performance of HEMT, it is effective to reduce the capacitance between the gate and source electrodes (C_{gs}), and so it is essential to reduce the gate length (L_g). The EB exposure method is known as one of the most effective methods of reducing L_g. If the gate pattern is drawn directly one by one on the wafer with an electron beam, the throughput is much lower than by i-line stepper exposure which can expose multiple gate patterns on the wafer in a batch, so it is very difficult to respond flexibly to fluctuations in production number. The side wall process or the thermal flow process has been proposed as a fine pattern forming method not using EB lithography(1) (2). In these processes, however, it is not easy to form L_g uniformly. To greatly improve the throughput, we developed a process technology which forms the short L_g gate electrode without using EB lithography, by combining i-line stepper exposure and the chemical shrink process. This paper describes the developed process technology and L_g variation and characteristics of prototype high electron mobility transistors (HEMTs).

2. Experiment Method

As a substitute for fine resist pattern forming by the EB lithography, we focused on a method that combines i-line stepper exposure with the chemical shrink process. Figure 1 shows the sequence of this chemical shrink process. First, the resist pattern is formed by i-line stepper exposure (Fig. 1a). Then, cross-linking reaction with the remaining acid at the resist trench occurs, and the shrink material which grows on the resist is coated on the resist surface (Fig. 1b). Subsequently, baking (Fig. 1c) causes the cross-linking reaction of the boundary layer between the shrink material and the resist, resulting in reduction of the resist trench. Lastly, the non-grown part of the shrink material is dissolved by pure water and removed (Fig. 1d). With this process, the resist pattern can be reduced to the resolution limit or less of the i-line stepper. In addition, by repeating the shrink process from Fig. 1 (b) to Fig. 1 (d), the resist pattern can be reduced to the desired width.

The method using both EB lithography and the chemical shrink process produced the gate electrode targeting L_g = 0.2 μm (hereafter, HEMTs produced by conventional EB lithography are called “EB lithography” and those produced using the newly developed chemical shrink process are called “chemical shrink process”). For the chemical shrink process, the cross-section of the resist pattern and the gate electrode was observed by scanning electron microscopy (SEM). The distribution of L_g on the surface was measured for both the EB lithography and the chemical shrink process. S-parameters of HEMTs were measured and ∠S11, noise

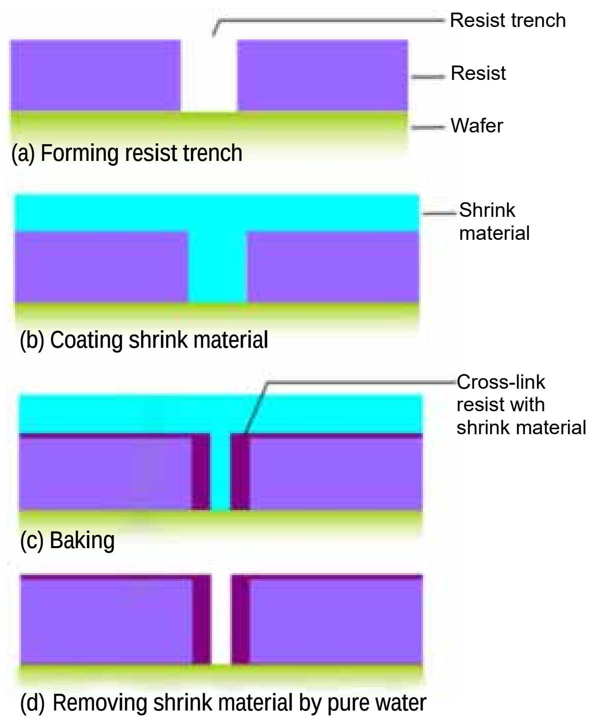

Fig. 1 Sequences of the chemical shrink process

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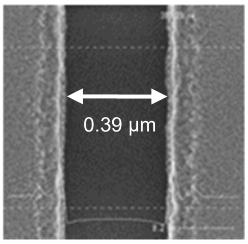
figure (NF) and associated gain (G_s) of S-parameters were evaluated. To evaluate the reliability, the high-temperature DC operating life test (test conditions: drain to source voltage (V_{ds}) = 3 V, drain current (Id) = 133.3 mA/mm, ambient temperature (T_a) = 125°C, time = 1000 hrs) was performed.

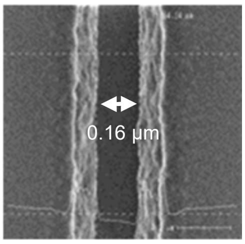
3. Experiment Result

3.1 Improvement of throughput

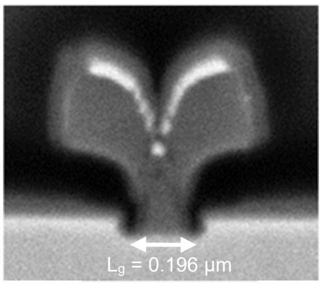
After measuring the throughput of the EB lithography and the chemical shrink process, we confirmed that the throughput of the chemical shrink process was 4.5 times faster than that of EB lithography.



(a) SEM images of resist trench before shrink process



(b) SEM images of resist trench after shrink process



(c) A cross-sectional image of gate

Fig. 2 SEM images of resist trench and gate electrode

3.2 SEM observation result

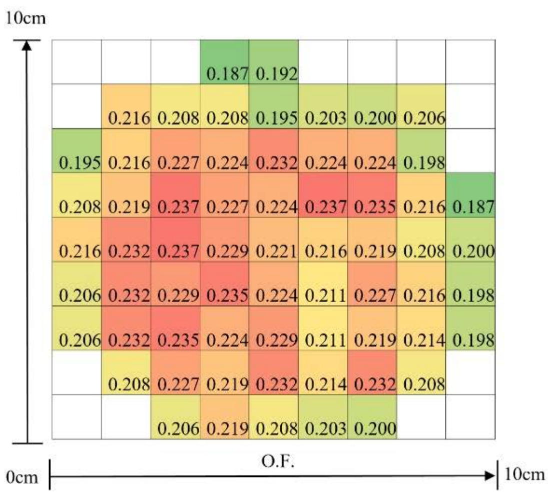
Figure 2 shows an SEM image of the resist trench and the gate electrode with the chemical shrink process. Figures 2 (a) and (b) are SEM images for measuring the length at the trench before and after the chemical shrink process. Several repetitions of the chemical shrink process reduced the trench from 0.39 μm to 0.16 μm. There was no residual resist at the trench and no poor formation after shrinking, and a good pattern shape was obtained. Figure 2 (c) is a cross-sectional SEM image of the gate electrode of the chemical shrink process and the electrode shape is equivalent to the gate electrode of the EB lithography. Forming was then performed to the desired length of L_g = 0.196 μm.

3.3 L_g variation

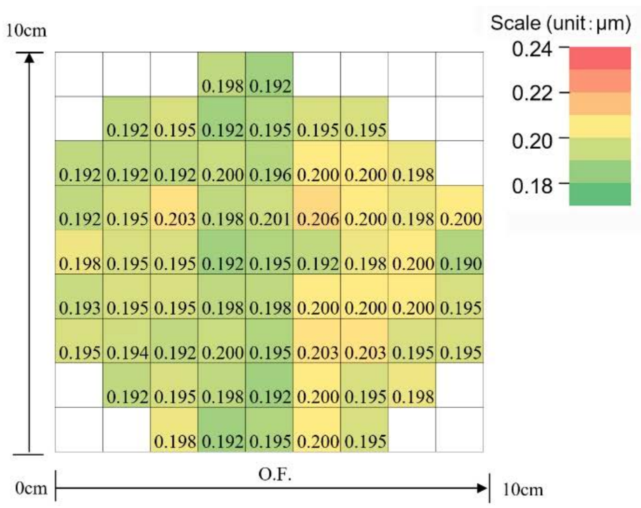
Figure 3 shows the L_g distribution wafer map of the EB lithography (Fig. 3a) and the chemical shrink process (Fig. 3b). The L_g average value and 3σ of the EB lithography were 0.216 μm and 0.040 μm. L_g at the edge of the wafer was shorter than at the center of the wafer. In contrast, the L_g average value and 3σ of the chemical shrink process were 0.196 μm and 0.010 μm. Dimensional variation was smaller for the chemical shrink process and L_g on the wafer surface was uniform.

3.4 Characteristic results of HEMTs

Figure 4 shows characteristic (∠S11, NF and G_s) results of the EB lithography and the chemical shrink process. In general, if L_g is short, C_{gs} is lowered, and ∠S11 and G_s become large and NF becomes small. Since the L_g average value was smaller for the chemical shrink process than the part of the EB lithography, the average of each characteristic value changed in a similar way. The L_g variation was small for the chemical shrink process, and the variation of each characteristic value was smaller for the chemical shrink process than the EB

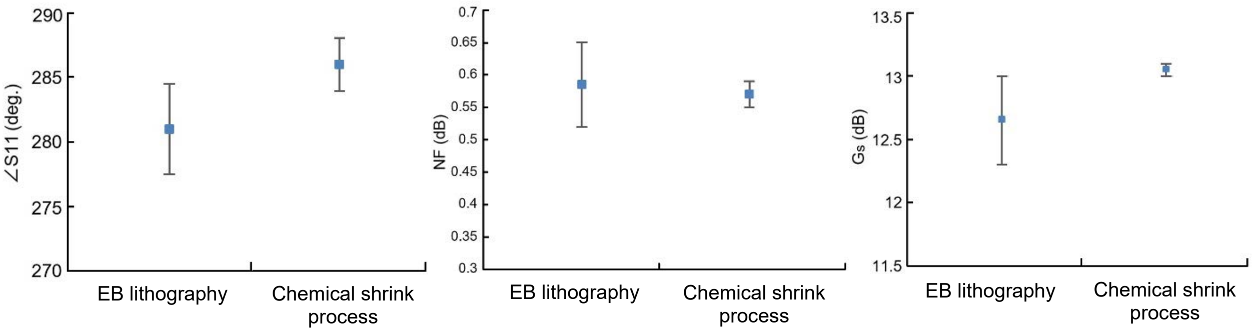


(a) EB lithography



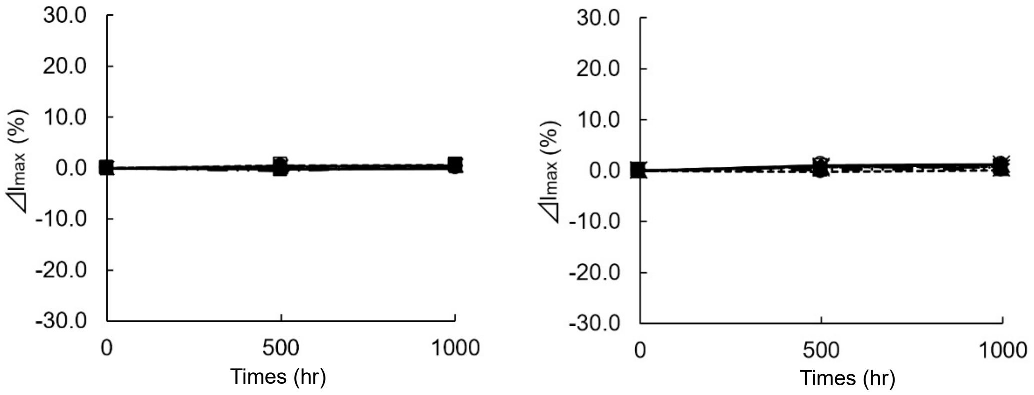
(b) Chemical shrink process

Fig. 3 Wafer map of L_g formed



(a) ∠S11 (b) NF (c) G_s

Fig. 4 Characteristics (∠S11, NF, G_s) for HEMT



(a) EB lithography (b) Chemical shrink process

Fig. 5 Rate of change of I_{max}

lithography. These results are equivalent to the electrical characteristics. It shows that the chemical shrink process has less variation, and that the developed chemical shrink process is effective.

Figure 5 shows the result of the rate of change of the saturated drain current (ΔI_{max}) of the HEMT high-temperature DC operating life test. After 500 and 1000 hours, ΔI_{max} was not changed for the EB lithography product or the chemical shrink process. The rate of change of the saturated drain current (I_{dss}) or the gate to source cut-off voltage (V_p) was also low and acceptable results in actual operation were obtained. From these results, HEMT formed by EB lithography and the chemical shrink process are equivalent in characteristics and reliability.

4. Conclusion

We developed a technology for forming a short gate which combines i-line stepper exposure with the chemical shrink process. Using this technology, a gate pattern of L_g = 0.196 μm was formed. Its variation (3σ) was 0.010 μm, which is very small compared to 0.040 μm of the EB exposure product, and the throughput was 4.5 times higher than by EB exposure. Evaluation of the characteristics and reliability showed equivalent characteristics to those of the EB exposure product. By using the newly developed technology, we will contribute to the reduction of product lead time and improve high-speed performance by using shorter L_g in the future.

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