Short-Gate Formation Process for High Throughput Production of GaAs-HEMT

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As a substitute for fine resist pattern forming by electron beam (EB) lithography, we developed a method of forming fine resist patterns with high throughput, by combining i-line stepper exposure with the chemical shrink process. A resist trench of 0.39 μm was formed from the i-line stepper and the trench was reduced to 0.16 μm by the chemical shrink process. Using this process, we successfully formed a uniform L_g = 0.196 μm gate electrode.

1. Background

GaAs HEMT has excellent high-speed performance and low noise characteristics, and is widely used in micro- and milli-wave devices such as for satellite broadcasting, in-vehicle radar, etc. To improve the high-speed performance of HEMT, it is effective to reduce the capacitance between the gate and source electrodes (C_{gs}), and so it is essential to reduce the gate length (L_g). The EB exposure method is known as one of the most effective methods of reducing L_g. If the gate pattern is drawn directly one by one on the wafer with an electron beam, the throughput is much lower than by i-line stepper exposure which can expose multiple gate patterns on the wafer in a batch, so it is very difficult to respond flexibly to fluctuations in production number. The side wall process or the thermal flow process has been proposed as a fine pattern forming method not using EB lithography[1][2]. In these processes, however, it is not easy to form L_g uniformly. To greatly improve the throughput, we developed a process technology which forms the short L_g gate electrode without using EB lithography, by combining i-line stepper exposure and the chemical shrink process. This paper describes the developed process technology and L_g variation and characteristics of prototype high electron mobility transistors (HEMTs).

2. Experiment Method

As a substitute for fine resist pattern forming by the EB lithography, we focused on a method that combines i-line stepper exposure with the chemical shrink process. Figure 1 shows the sequence of this chemical shrink process. First, the resist pattern is formed by i-line stepper exposure (Fig. 1a). Then, cross-linking reaction with the remaining acid at the resist trench occurs, and the shrink material which grows on the resist is coated on the resist surface (Fig. 1b). Subsequently, baking (Fig. 1c) causes the cross-linking reaction of the boundary layer between the shrink material and the resist, resulting in reduction of the resist trench. Lastly, the non-grown part of the shrink material is dissolved by pure water and removed (Fig. 1d). With this process, the resist pattern can be reduced to the resolution limit or less of the i-line stepper. In addition, by repeating the shrink process from Fig. 1 (b) to Fig. 1 (d), the resist pattern can be reduced to the desired width.

The method using both EB lithography and the chemical shrink process produced the gate electrode targeting L_g = 0.2 μm (hereafter, HEMTs produced by conventional EB lithography are called "EB lithography" and those produced using the newly developed chemical shrink process are called "chemical shrink process"). For the chemical shrink process, the cross-section of the resist pattern and the gate electrode was observed by scanning electron microscopy (SEM). The distribution of L_g on the surface was measured for both the EB lithography and the chemical shrink process. S-parameters of HEMTs were measured and ∠S11, noise

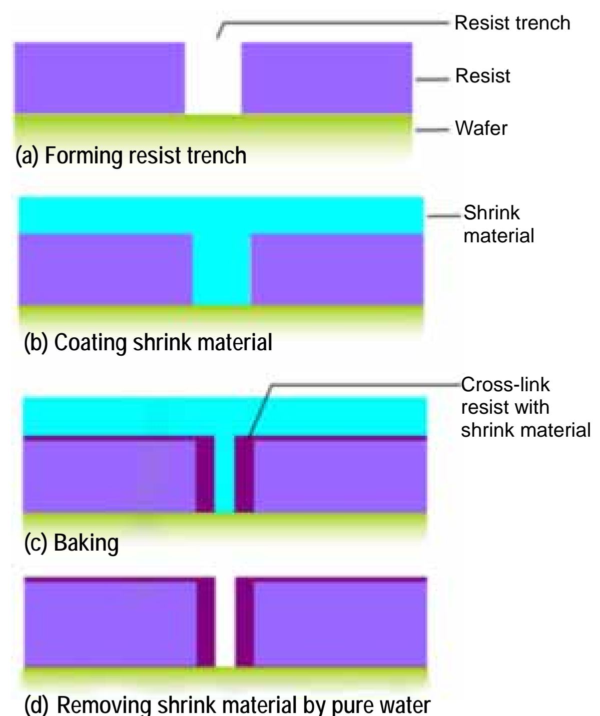

Fig. 1 Sequences of the chemical shrink process

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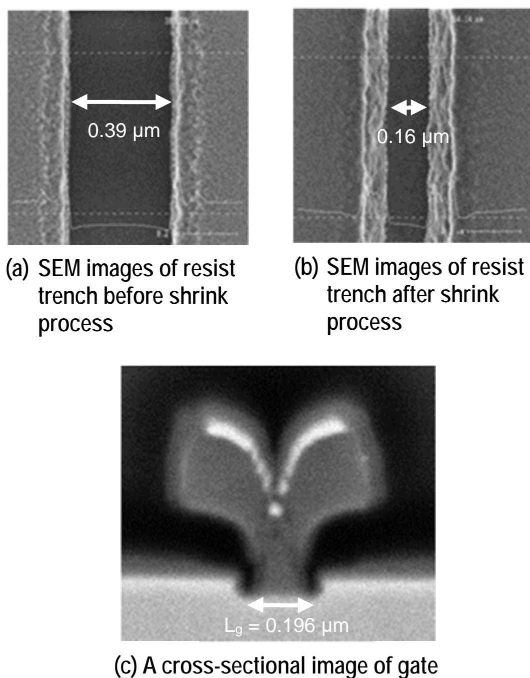
figure (NF) and associated gain (G_s) of S-parameters were evaluated. To evaluate the reliability, the high-temperature DC operating life test (test conditions: drain to source voltage (V_{ds}) = 3 V, drain current (Id) = 133.3 mA/mm, ambient temperature (T_a) = 125°C, time = 1000 hrs) was performed.

3. Experiment Result

3.1 Improvement of throughput

After measuring the throughput of the EB lithography and the chemical shrink process, we confirmed that the throughput of the chemical shrink process was 4.5 times faster than that of EB lithography.



(a) SEM images of resist trench before shrink process

(b) SEM images of resist trench after shrink process

(c) A cross-sectional image of gate

Fig. 2 SEM images of resist trench and gate electrode

3.2 SEM observation result

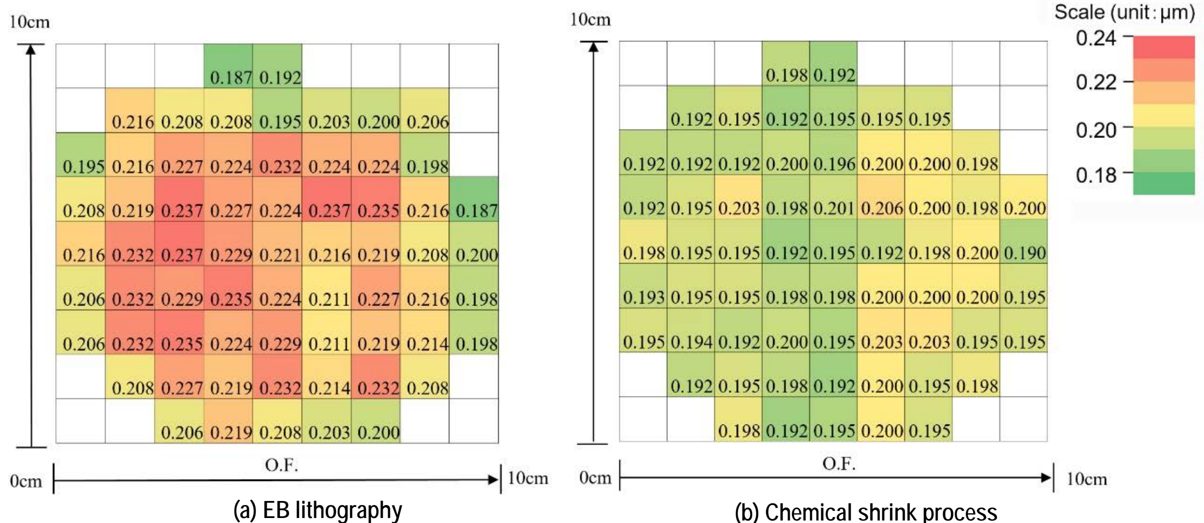
Figure 2 shows an SEM image of the resist trench and the gate electrode with the chemical shrink process. Figures 2 (a) and (b) are SEM images for measuring the length at the trench before and after the chemical shrink process. Several repetitions of the chemical shrink process reduced the trench from 0.39 µm to 0.16 µm. There was no residual resist at the trench and no poor formation after shrinking, and a good pattern shape was obtained. Figure 2 (c) is a cross-sectional SEM image of the gate electrode of the chemical shrink process and the electrode shape is equivalent to the gate electrode of the EB lithography. Forming was then performed to the desired length of L_g = 0.196 µm.

3.3 L_g variation

Figure 3 shows the L_g distribution wafer map of the EB lithography (Fig. 3a) and the chemical shrink process (Fig. 3b). The L_g average value and 3σ of the EB lithography were 0.216 µm and 0.040 µm. L_g at the edge of the wafer was shorter than at the center of the wafer. In contrast, the L_g average value and 3σ of the chemical shrink process were 0.196 µm and 0.010 µm. Dimensional variation was smaller for the chemical shrink process and L_g on the wafer surface was uniform.

3.4 Characteristic results of HEMTs

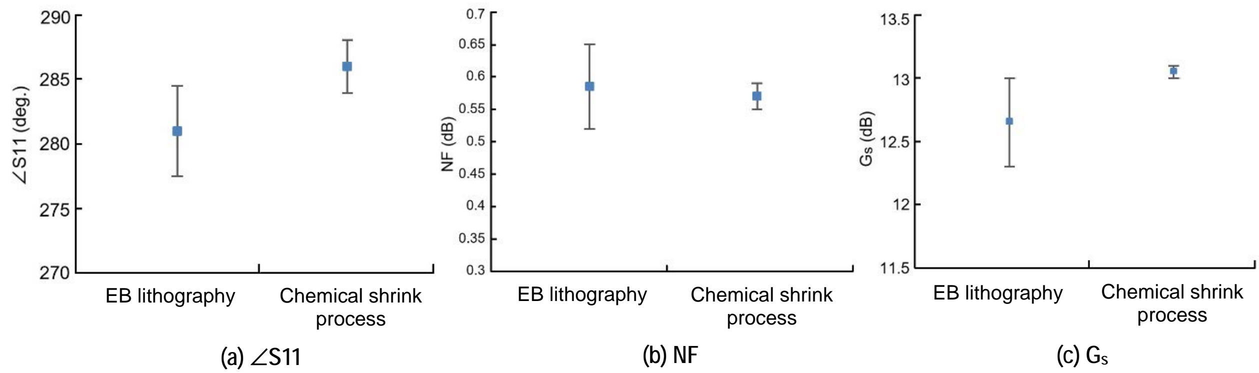
Figure 4 shows characteristic (∠S11, NF and G_s) results of the EB lithography and the chemical shrink process. In general, if L_g is short, C_{gs} is lowered, and ∠S11 and G_s become large and NF becomes small. Since the L_g average value was smaller for the chemical shrink process than the part of the EB lithography, the average of each characteristic value changed in a similar way. The L_g variation was small for the chemical shrink process, and the variation of each characteristic value was smaller for the chemical shrink process than the EB



(a) EB lithography

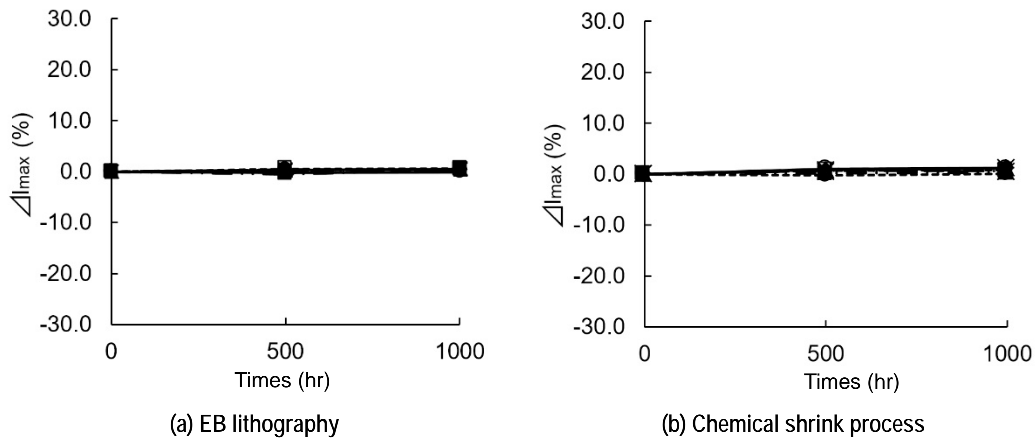
(b) Chemical shrink process

Fig. 3 Wafer map of L_g formed



(a) ∠S11 (b) NF (c) G_s

Fig. 4 Characteristics (∠S11, NF, G_s) for HEMT



(a) EB lithography (b) Chemical shrink process

Fig. 5 Rate of change of I_{max}

lithography. These results are equivalent to the electrical characteristics. It shows that the chemical shrink process has less variation, and that the developed chemical shrink process is effective.

Figure 5 shows the result of the rate of change of the saturated drain current (ΔI_{max}) of the HEMT high-temperature DC operating life test. After 500 and 1000 hours, ΔI_{max} was not changed for the EB lithography product or the chemical shrink process. The rate of change of the saturated drain current (I_{dss}) or the gate to source cut-off voltage (V_p) was also low and acceptable results in actual operation were obtained. From these results, HEMT formed by EB lithography and the chemical shrink process are equivalent in characteristics and reliability.

4. Conclusion

We developed a technology for forming a short gate which combines i-line stepper exposure with the chemical shrink process. Using this technology, a gate pattern of L_g = 0.196 μm was formed. Its variation (3σ) was 0.010 μm, which is very small compared to 0.040 μm of the EB exposure product, and the throughput was 4.5 times higher than by EB exposure. Evaluation of the characteristics and reliability showed equivalent characteristics to those of the EB exposure product. By using the newly developed technology, we will contribute to the reduction of product lead time and improve high-speed performance by using shorter L_g in the future.

5. References

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