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Edition on Power Devices to Support Tomorrow's Society

MITSUBISHI ELECTRIC
Changes for the Better

A Quarterly Survey of New Products, Systems, and Technology

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Edition on Power Devices to Support Tomorrow's Society

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Cover Story
Mitsubishi Electric's Power Devices Protect the Environment.
In recent years, inverter equipment has been increasingly adopted on environmental considerations because it offers not only reduced energy consumption but is also attracting attention as the key to securing clean energy sources such as wind power and solar power. Mitsubishi Electric creates and supplies power devices ideal for this inverter equipment in the multiplicity of uses to which it is put. Our cover shows representative products from this range against a backdrop of the world whose environment they help to protect.

Editorial Inquiries

Keizo Hama
Corporate Total Productivity Management & Environmental Programs
Fax 03-3218-2465

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Product Inquiries

CHINA
Keling Electric (Shanghai) Co., Ltd.
39th Floor, Shanghai Senmao International Building,
101 Yin Cheng East Road,
Pudong New Area, Shanghai, P.R.C.
Qian Yu Feng
Tel 21-6841-5300
Fax 21-6841-0100

NORTH AMERICA
POWEREX WORLDWIDE
POWER SEMICONDUCTOR
SALES AND MARKETING HEADQUARTERS
Youngwood, Pennsylvania Powerex, Inc.
200E. Hillis Street, Youngwood, PA 15697-1800
Ron Williams
Tel 724-9425-7272
Fax 724-925-4393
http://www.pwrx.com

GERMANY
Mitsubishi Electric Europe B.V.
German Branch
Gothaer Strasse 8
D-4030 Ratingen 1, Germany
Robert Wiatr
Tel 2102-486-0
Fax 2102-486-367

Overview

Advances in Power Devices to Support Tomorrow's Society

*by Yasuji Nagayama**

In the 21st century, when so much attention is being concentrated on environmental issues, advances in reducing energy consumption and in clean energy have an essential part to play in measures to reduce the volume of CO_2 generated. Central to these efforts are energy-efficient electrical equipment, as typified by inverters, and solar and wind power among other clean sources of energy. It is here, in the conversion of electrical power, that power semiconductor devices will play the crucial role. They are literally indispensable.

Mitsubishi Electric Corporation, as a leading manufacturer of these devices, boasts a research and development organization that successfully implements our corporate vision–to use technological innovation to launch new products and create new markets relying upon integrated expertise not only in semiconductor processes but also in package development and applications. The IGBT, the power chip at the heart of so many of these devices, is now taking prodigious strides in reduced losses thanks to the development of trench structures, and is making major contributions to energy saving. Higher integration and intelligence are also creating new generations of devices that provide solutions. Our accumulated expertise in peripheral devices is also developing LVICs and HVICs that combine with power chips to create intelligent power modules (IPMs) based on entirely new concepts.

As these IGBT modules and IPMs advance from one generation to the next, they are creating new markets for the power modules of the future. This issue of *Advance* introduces some of the latest technologies and products in this vital field. ❑

**Yasuji Nagayama is General Manager of Power Device Works.*

The NF Series: New Trench-type IGBT Modules with Low Power Drive

*by Mitsuharu Tabata and Tooru Matsuoka**

The NF series features IGBT modules that use CSTBTs. CSTBTs, which surpass the theoretical barriers for IGBT performance, have the most advanced fundamental characteristics while still using essentially the same technology as conventional trench IGBTs. In planning NF Series products, ease of use and compatibility were considered, rather than focusing exclusively on reduction of losses. The NFH Series was developed at the same time for high-frequency switching applications.

The NF Series

Mitsubishi Electric Corporation has marketed dual-IGBT 100A to 600A IGBT modules containing CSTBTs, developed as the fifth-generation IGBT (see Table 1). This series serves the strong market demand for dual-element IGBT modules. The corporation's conventional H series product is used in a wide variety of applications, and many firms have developed a broad range of application technologies for these products. In order to take advantage of these existing technological resources while switching to state-of-the-art elements, the dual-element NF series features package dimensions (Fig. 1), drive characteristics, short-circuit characteristics, etc., similar to those of the H series. The CSTBTs should be thought of as an extension on the tried-and-true trench IGBT technologies, with improvements in terms of high reliability/stable supply design.

Based on the fourth-generation trench IGBT structure, this fifth-generation IGBT chip uses three superior technologies: the carrier stored trench-gate bipolar transistor (CSTBT) structure (providing improved performance), the plugging cell merged (PCM) technology (which controls the channel density), and the light punch through (LPT) structure (which facilitates parallel connections with high-voltage elements and facilitates faster switching, while improving failure capability or endurance). Each of these technologies is described below.

Fig. 1 NF Series and H Series: In each pair, the H Series unit is on the left and the NF Series unit is on the right.

The n^- drift layer resistance, which is high when the element is OFF in order to maintain the breakdown voltage, is reduced by the injection of holes from the P collector region when the element is ON. The concentration of these holes falls with the distance from the injection point, so the resistance tends to remain high in the vicinity of the emitter. CSTBT is a technology in which innovations have increased the concentration of holes in the vicinity of the emitter.

On the other hand, even though trench IGBTs have the advantage of providing extremely high current densities, this characteristic becomes a

Table 1 Product Line (all products have dual elements)

Series	Vces (V)	Ic(A)					
		100	150	200	300	400	500
NF	600	-	CM150DY-12NF	CM200DY-12NF	CM300DY-12NF	CM400DY-12NF	CM400DY-12NF
	1200	CM100DY-24NF	CM150DY-24NF	CM200DY-24NF	CM300DY-24NF	CM400DY-24NF	CM500DY-24NF
NFH	600	-	-	CM200DU-12NFH	CM300DU-12NFH	CM400DU-12NFH	CM500DU-12NFH
	1200	CM100DU-24NFH	CM150DU-24NFH	CM200DU-24NFH	CM300DU-24NFH	CM400DU-24NFH	CM500DU-24NFH

**Mitsuharu Tabata and Tooru Matsuoka are with the Power Device Works.*

disadvantage in applications that require short-circuit capabilities. While short-circuit capabilities require the channel density to be reduced, simply expanding the gap between trenches has an impact on the withstand voltage. Given this, PCM technology fills in the trench gates for one out of every few trenches, causing the gate to short to the emitter to prevent operation. This makes it possible to obtain input capacitance characteristics and short-circuit capabilities similar to those of planar IGBTs.

The structures of IGBTs can be categorized as punch-through (PT) or non-punch-through (NPT) structures. Generally, PT structures, with their lower saturation voltage, are particularly effective for low withstand voltage applications, while NPT structures are more suitable for higher withstand voltages, where switching losses are a larger proportion of total losses and lower saturation voltages matter less.The light punch-through (LPT) structure is positioned between them, and is used in 1,200V-class IGBTs.

Because this product series is compatible with the H series, the rated currents (model names) are set in a way markedly different from general products. The CSTBT is a descendant of the trench IGBT, with an extremely low saturation voltage and high DC current-carrying capabilities; however, in many 1,200V applications where switching losses predominate, when the rated current is set by the DC current-carrying capability, problems arise in terms of compatibility with the H series. To ensure compatibility with units in the H series that have the same rated current for that type name, the margin in the NF series is about one rank above that which is usual for the current-carrying capability. While this causes a shift in the current-carrying capability ranking in the direction of having too large a margin for new designs, which often have lower switching frequencies, this approach was adopted to ensure compatibility with the H series.

On the other hand, in the later part of the third generation products, the corporation made major improvements in packaging (specifically in the U and F Series). The power-cycling life expectancy was improved dramatically through the move to a single soldering cycle and through the selection of the optimal solder. The NF series from now on uses packages with improved internal structures while maintaining compatibility with the third-generation IGBT in terms of external dimensions (Fig. 2), and power-cycling life expectancies have again been improved dramatically through the optimization of the wire-bonding conditions and parameters (Fig. 3). Similarly, major improvements in the later part of the third generation dramatically decreased the stray inductance of the main terminal parts, and, based on this technology, the NF series has succeeded in reducing the inductance by about half that of the H Series, while still maintaining compatibility with the H Series' dimensions.

Fig. 2 An H Series-compatible cover on an F Series base case equals NF Series

The NFH Series

The corporation has also marketed the NFH series of IGBT modules, taking advantage of broad latitude in adjusting the carrier density spread in the CSTBT structures to increase the turnoff speeds of the elements (see Table 1 and Fig. 4). The 30~60kHz circuitry, and the H bridge circuit in particular, have been adjusted, targeting applications such as medical equipment, induction heating, welding equipment, high-frequency power links, etc., equipment that involves turn-on soft switching and turn-off hard switching. The turnoff speed for general-use IGBTs is rather slow, making them difficult to use in these applications. In particular, the low-noise countermeasures of recent IGBT modules often counter the requirements for high-fre-

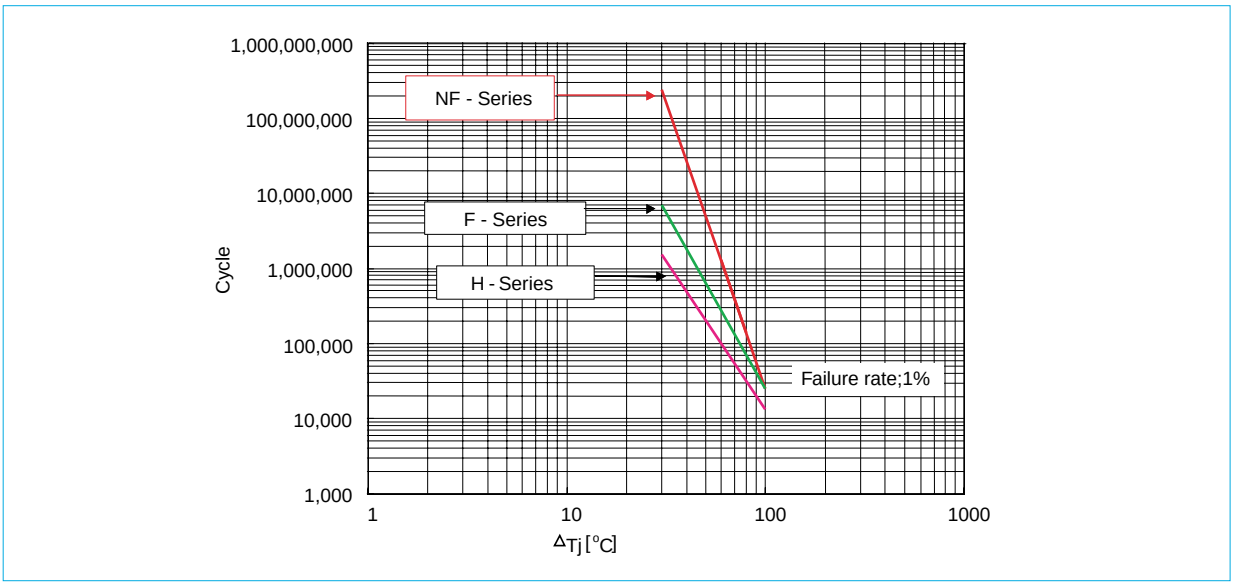


Fig. 3 Power-cycle compatibility

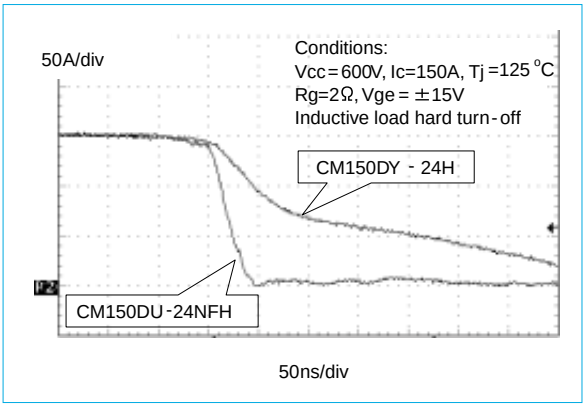


Fig. 4 Comparison of turnoff waveforms for the NFH Series and the H Series

quency responsiveness. Generally, when minority carrier lifetimes are reduced excessively in order to provide high-speed response in IGBTs the on-state voltage drop will be extremely high due to the reduction in modulation in the n- layer at lower currents. However, this phenomenon is less likely in the LPT structure used in the CSTBTs for the 1,200V Class.

Based on the U and F series packages, with their reduced stray inductances, the NFH series takes the skin effect into account in strengthening the internal interconnections. The rated current, freewheeling diode, outline, etc., have been set independently in accordance with the fact that the NFH Series' IGBTs are used in applications that are very different from those of standard IGBT modules. The NFH Series of IGBT modules gives preference to switching speed over short-circuit capabilities. In this way, the NFH series specializes in high-speed turn-off characteristics, and even though losses are small, this series is not intended for general inverter applications, but rather can be used to pursue performance that has been difficult to achieve with conventional IGBT modules in high-frequency switching applications.

The new NF series, by incorporating the very latest technical developments while maintaining the greatest possible compatibility with the previous generation, ensure that the many companies using Mitsubishi Electric's products will be readily able to make the transition to take advantage of the superior performance offered with the minimum disclocation of their production lines. The NF and NFH series will also open up new applications where their superior performance will offer significant competitive advantages. ❑

L Series IPMs: Low Loss, Low Noise, New Control

*by Nobutake Taniguchi and Takahiro Inoue**

The newly developed Mitsubishi Electric Corporation L Series intelligent power modules (IPMs) feature a new, smaller package, and have reduced losses due to the use of a fifth-generation IGBT (the CSTBT), and reduced noise due to a newly developed control/driving circuitry. Typical packages are shown in Fig. 1 and their dimensions, etc., in Fig. 2.

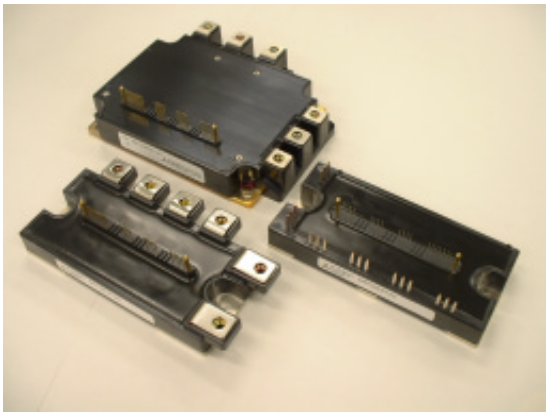


Fig. 1 The L Series 5th-generation IPMs

Chip Technologies

To reduce losses, the L Series IPM uses a carrier-stored trench-gate bipolar transistor (a CSTBT) fifth-generation IGBT in a fifth-generation IPM circuit. The CSTBT is a leading-edge power chip that provides an excellent trade-off between low "on" voltages and the IGBT turn off loss.

To reduce noise in the forward direction, the new IPM uses the same lifetime-control technology as in the fourth-generation intelligent power module.

The use of these leading-edge power chips, in combination with the new control/driving methods described below, constitutes a fifth-generation IPM with significantly reduces losses and noise.

CONTROL CIRCUIT TECHNOLOGY. Although reduced switching losses are often associated with increased electromagnetic interference noise, and, conversely, reduced electromagnetic interference often means increased switching losses, the IGBT control/drive method was reviewed and new control ICs were developed in order to provide this fifth-generation IPM with superior performance in both of these areas.

In the conventional control-circuit approach, used up to and including the fourth-generation S-DASH IPMs, the parameters that determine the switching speed (that is, the output voltage,

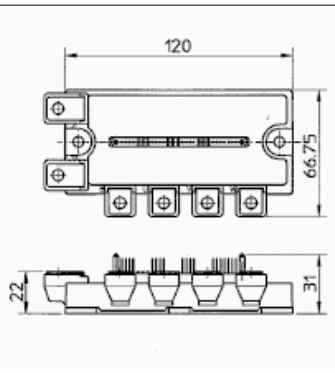
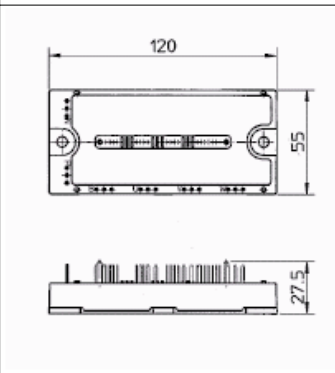
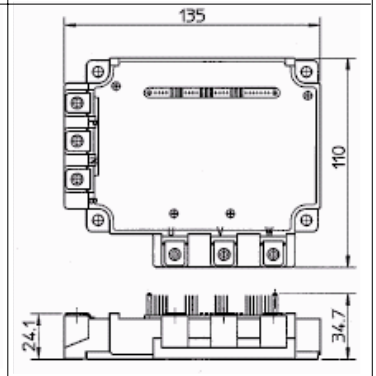
Package type	Type A (Terminal screw type)	Type B (Terminal solder type)	Type C (Terminal screw type)
Shape			
LxWxH(mm)	66.75x120x31	55x120x27.5	110x135x34.7
Weight(g)	380	340	800

Fig. 2 Dimensions of the 5th-generation IPM package types

* *Nobutake Taniguchi and Takahiro Inoue are with Power Device Works.*

gate resistance Rg, etc., of the control IC) could not be changed. Because of this, setting the switching speed so as to reduce the electromagnetic interference would have the drawback of increasing losses in all electrical current domains.

In contrast, the switching speed in the new power-module circuits can be toggled between two levels by the IGBT collector current. Fig. 3 is a block diagram of this fifth-generation IPM

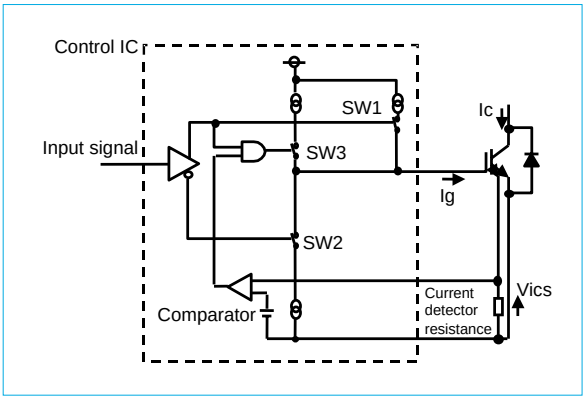


Fig. 3 Control circuit for the 5th-generation IPM

control circuit, and Fig. 4 is a time chart for the control circuit. In the figures, V_{IN} is the control input signal, I_c is the collector current, V_{ics} is the collector-current detector voltage, and I_g is the gate-drive current. If the collector current I_c is less than the current value that would switch the switching speed, the IGBT is driven by only a single current source (SW1: ON, SW3: OFF), but when the collector current I_c is higher than the current value for switching, the IGBT is driven by two current sources SW1 and SW3 are both ON).

Consequently, the gate voltage rises more gradually in the low-current domain, resulting in "soft switching" and making it possible to reduce the electromagnetic interference noise by reducing the *dv/dt* turn-off in the forward direction. On the other hand, in the high-current

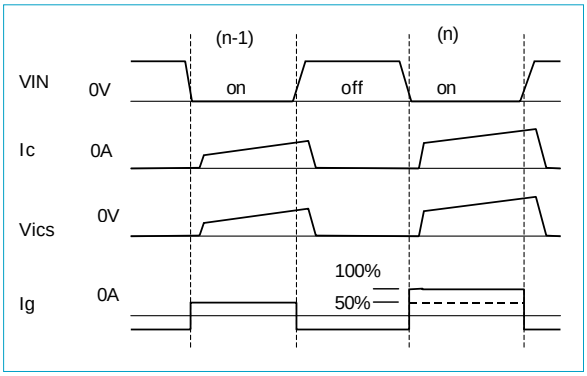


Fig. 4 Control-circuit timing chart

domain, the switching is done at the normal speed, making it possible to reduce losses.

Fig. 5 shows the *dv/dt* collector-current dependency when turning off in the forward direction, with and without this soft switching. In the low-current domain, the soft switching is able to reduce the *dv/dt* when there is a forward-direction turnoff.

Fig. 6 shows the V_{EC} waveform when turning off in the forward direction, with and without the soft switching. This succeeds in reducing the forward-direction turnoff *dv/dt* when the IGBT is turned off. Fig. 7 shows the results of measuring radio-frequency noise when a motor is actually running, using a fourth-generation intelligent power module versus the new, fifth-

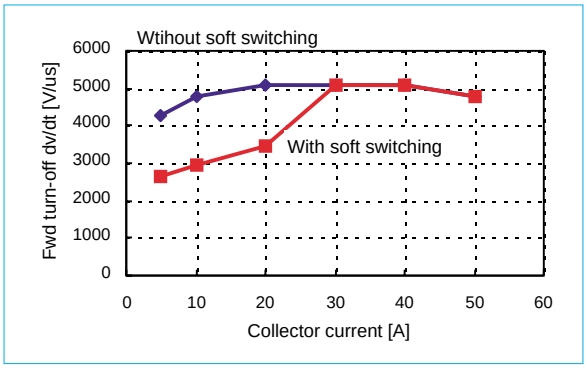


Fig. 5 Relationship between dv/dt *and the collector current in forward turnoff*

generation module. This noise is reduced by approximately 10dB. The above approach successfully provided a control-circuit method that reduces both losses noise in the new module.

PACKAGING TECHNOLOGY. Three new types of packages have been developed for the fifth-generation intelligent power module. These packages are as shown in Fig. 1 and 2.

Ratings from 50~300A/600V and 25~150A/1,200V are covered by two packages-a screw-type primary terminal shape (A and C in Fig. 2). The range of choices offered to the customer is increased by the product line including one package, with a pin-type primary terminal shape, for the 50~75A/600V and 25~75 A/1,200V range (the B type in Fig. 2).

The fifth-generation packages are about 32% smaller than the fourth-generation IPMs (the S-DASH series) in terms of the mounting surface area of the packages in the 50~150A/ 600V and 50~75A/1,200V (types A and B in Fig. 1) due to aggressive package size and weight reductions achieved by optimizing the chip layout and the positions of the electrode contacts.

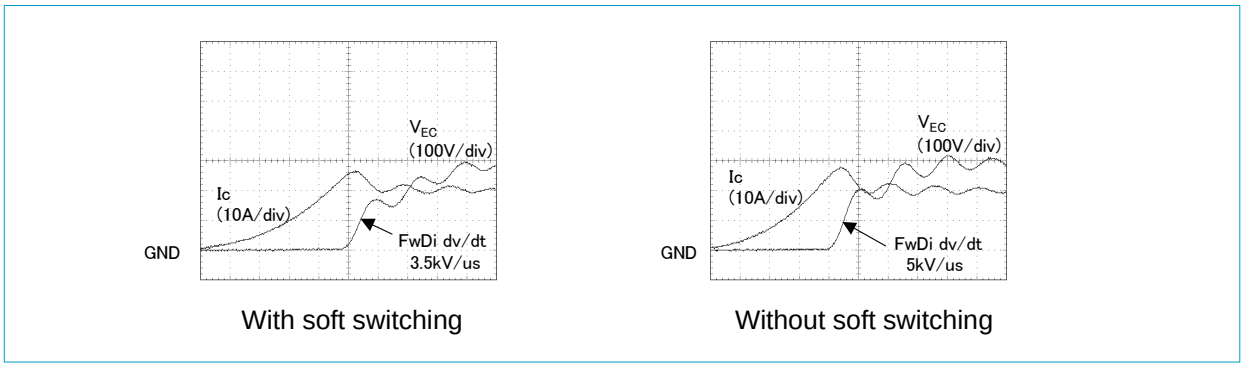


Fig. 6 Relationship between dv/dt *and the collector current in forward turnoff*

Table 1 Fifth-Generation IPM Product Lineup

Available variants, ratings and product numbers.			Rated current Ic (A) and collector loss (W)				Package type
Motor rating	Model number	Rated Voltage	Inverter section		Brake section		
3.75kW	PM50RLA060	600V	50W	131W	30A	103W	A
	PM50RLB060						B
5.5/7.5kW	PM75RLA060		75A	390W	50A	297W	A
	PM75RLB060						B
11kW	PM100RLA060		100A	462W	50A	297W	A
15/18.5kW	PM150RLA060		150A	625W	75A	390W	A
22kW	PM200RLA060		200A	781W	100A	462W	C
30kW	PM300RLA060		300A	1041W	150A	625W	C
3.7kW	PM25RLA120	1200V	25A	150W	15A	130W	A
	PM25RLB120						B
5.5/7.5kW	PM50RLA120		50A	480W	25A	347W	A
	PM25RLB120						B
11/15kW	PM75RLA120		75A	595W	40A	446W	A
	PM75RLB120						B
16/18.5kW	PM100RLA120		100A	781W	50A	480W	C
30kW	PM150RLA120		150A	1041W	75A	595W	C

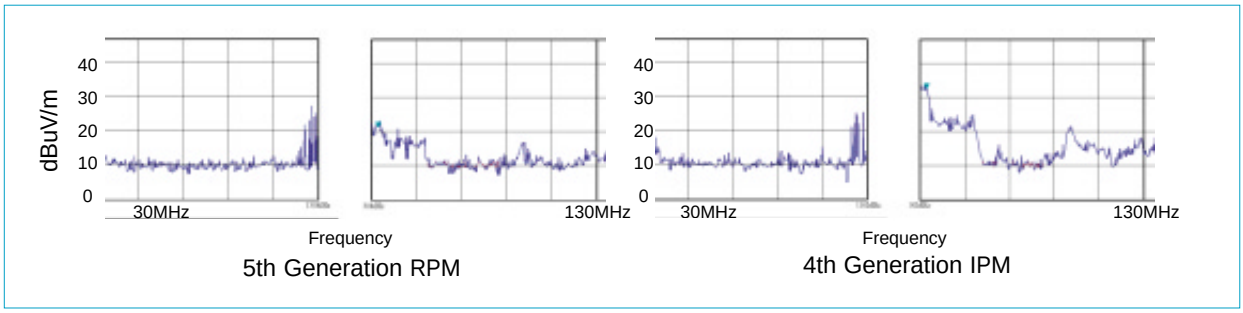


Fig. 7 Comparisons of EMI noise in an IPM rated 50A/600V (time axis equals 50ns per div.) (Conditions: Vcc = 300V, Carrier Frequency = 4kHz, Output Current = 17A (rms), Dead Time = 5μs)

For the 200~300A/600V and 100~150A/1,200V packages (type C in Fig. 1), the primary and control terminal positions are identical to those of the fourth-generation S-DASH series, where the substrate size is reduced while maintaining geometric interchangeability with the previous generation.

In terms of improvements in previously irreconcilable parameters, in overall performance, and packing technologies that ensure reduced size and compatability with the previous generation, these new IPMs will contribute significantly to higher performance in smaller, lighter power equipment. ❑

High-Capacity Dual-Element IGBT Module: Mega Power Dual

*by Junji Yamada and Seiji Saiki**

The Mega Power Dual series is a series of high-capacity dual IGBT modules that provide both low losses and low noise through the provision of leading-edge CSTBTs and soft-recovery free wheel diodes. The module packages were developed specially to provide a compact, easy-to-use structure.

CSTBTs With The New PCM (Plugging-Cell Merged) Structure

CSTBTs have a structure with an additional n layer, relatively highly doped, between the p base layer and the n^- layer of a conventional trench IGBT. In the conventional trench IGBT, holes are injected into the n^- layer from the p^+ layer on the collector side, and pass through to the emitter side when the device is on. On the other hand, in a CSTBT, the impurity concentration in the n layer that forms a junction with the p base is higher than in the n^- layer, so the intrinsic junction voltage at the p base-n junction is about 0.2 volts higher than the junction voltage for the p base-n^- junction in the conventional trench IGBT. As is shown in Fig. 1a, this junction voltage is a barrier preventing the movement of holes from the n layer into the p base layer. In other words, because the n layer limits the movement of holes into the p base layer, the holes accumulate within the device. This charge accumulation function causes the distribution of the minority carrier holes in the CSTBT to be higher than in the conventional structure, as shown in Fig. 1b, and as a result, the ON voltage characteristics of the CSTBTs are substantially lower than in trench IGBTs. Furthermore, plugging-cell merged (PCM) CSTBTs, with a structure in which the embedded cells are partially merged, have lower input capacitances than trench IGBTs, and can be driven by gate-driver circuits on a par with conventional third-generation planar IGBT modules. In addition, because it is possible to control the $ICE_{(sat)}$, a short circuit capability of at least ten microseconds, the same as for the third-generation planar IGBT, has been secured, even without the use of an RTC circuit.

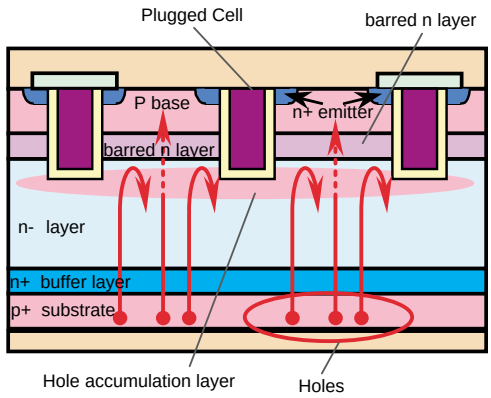


Fig. 1a

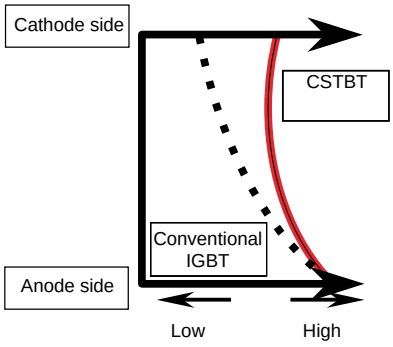


Fig. 1b

Fig. 1 CSTBT structure and characteristics

Soft Recovery Diodes

Although the noise that is generated during switching results from the external line impedance rather than from within the device itself, this noise can still be substantially attenuated by modifying the switching waveform of the device. In particular, the recovery of free-wheel diodes (FWDs) can soften the electric current oscillations that are generated by triggers, and so attenuate noise. The IGBT modules developed in this project take advantage of local carrier lifetime control in the FWDs to achieve rapid-yet-soft recovery characteristics without sacrificing a low forward voltage drop (VF) for the diode.

New MDP Packages

By overcoming the shortcomings of conventional

**Junji Yamada is with the Power Device Works and Seiji Saiki is with Fukuryo Semicon Engineering Corporation.*

packages and using a variety of new structures and new device technologies, Mitsubishi Electric Corporation has produced a package that is both compact and easy to use. These new technologies are described below.

SMALLER MODULES. Optimizing the multilayer interconnect structures and the distances between layers in the packages has made it possible to reduce the size and weight of devices through a dramatic almost 60% reduction in the module area, relative to a conventional (single-element) device with a rated current of 1,000 amps.

LOW-INDUCTANCE STRUCTURE. As is shown in Fig. 2, efforts to miniaturize the main electrode structures through the multilayer interconnections within the package itself, and efforts to minimize the insulation distance between opposite polarities to achieve an insulator 0.4mm thick, has made it possible to reduce the within-package inductance to about half that of conventional single-element 1,000-amp rated current devices.

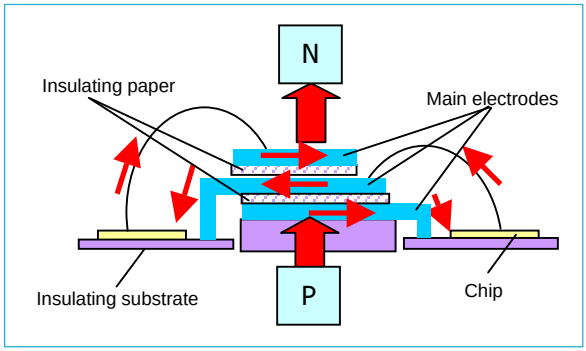


Fig. 2 Cross-sectional structure and current pathways of the main electrodes

SIMPLIFIED INTERCONNECTIONS. These use multihole step terminals. As shown in Fig. 3, the use of multihole step terminals, in which there is a step height in the p and n terminals, facilitates insulated-laminate parallel-plate connections. Additionally, 3M6 nuts are provided on each in order to secure an adequate contact area with an insulating-laminate parallel flat plate, and the use of the nuts without chamfering has doubled the contact surface with the insulating-laminate parallel flat plate compared with normal nuts.

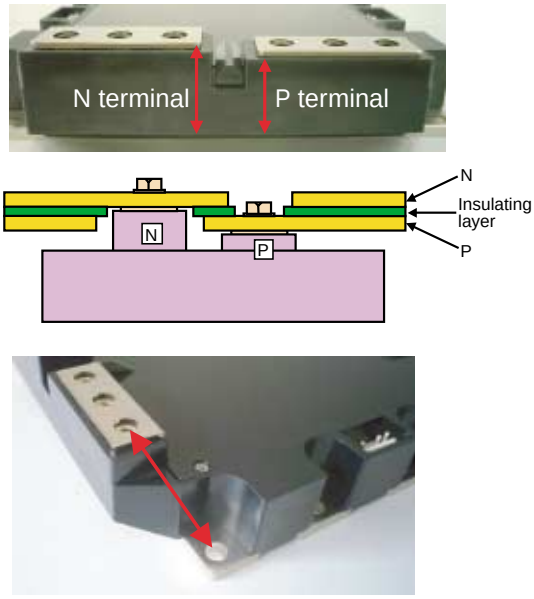


Fig. 3 Configuration of the step terminals and mounting holes

On the other hand, the provision of the P and N terminals on the ends makes it possible to reduce the insulating-laminate parallel-plate surface area, which is effective in improving the ease of assembly, reducing the weight of the device, reducing the interconnection inductance, etc. Furthermore, the design of the outputs and interconnections is simplified by locating the P and N terminals and the output terminals at opposite positions on the packages.

SEPARATING STEP TERMINALS AND MOUNTING HOLES. This increases the isolation. As shown in Fig. 3b, the mounting holes and step terminals that contact the insulating laminate parallel flat plate are separated for adequate isolation. For efficiency in assembly and replacement, the

mounting operations can be simplified by having the same bolt size (M6) for the terminals as for the mounting holes.

CONTROL TERMINAL CONNECTOR. As shown in Fig. 4, connectors to the gate terminal, the emitter sense terminal, and the connector-voltage detection terminal are used, which is very convenient for assembly and replacement. Two pins are used for each control terminal, and a locking structure is also used, thereby reducing the frequency of malfunctions due to contact failures. Other structures, such as countersinking the holes in the case in order to make it more difficult for contacts to become detached, are used to increase reliability.

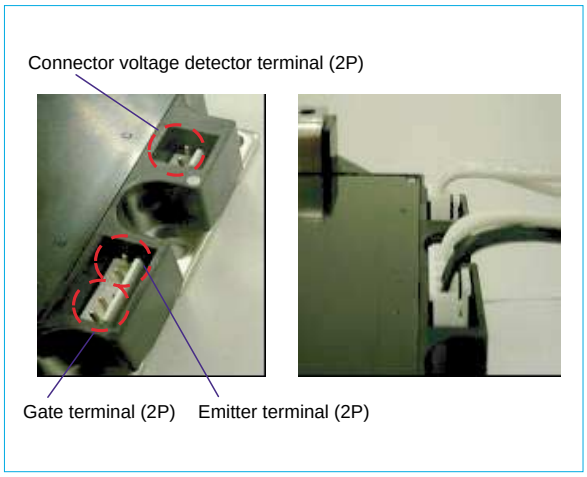


Fig. 4 Connector terminals

As shown in Fig. 5, the design of water-cooling fins and the cooling paths is simplified, being free of intersections between the mount holes and the ducting for water cooling because the chips and mount holes are structured parallel to the principle electrodes. Finally, the product line features three types of dual-element products, the 900A/1200V product, the 1400A/1200V product, and the 1000A/1700V product, facilitating use in a three-phase inverter with a single-unit capacity of between 300 and 460kVA.

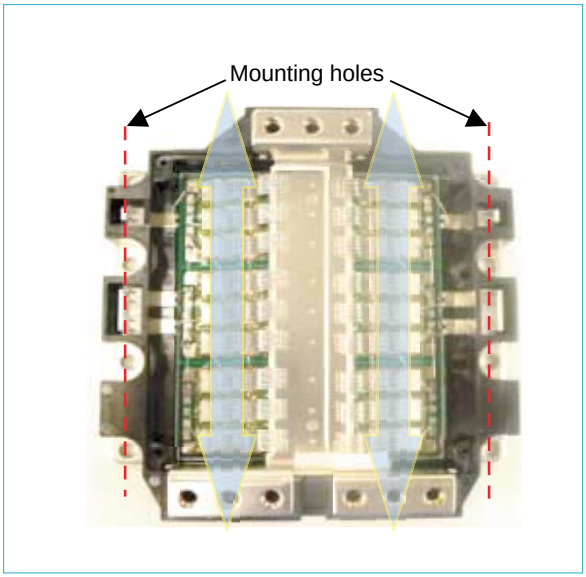


Fig. 5 Cooling pathway mounting holes

The advanced technology and improved performance of the modules introduced here, with their new packaging, ensure them a major role in the products and systems of the near future . ❑

Next-Generation DIP-IPMs Driven by 3V Microcontroller

*by Shinya Shirakawa and Touru Iwagami**

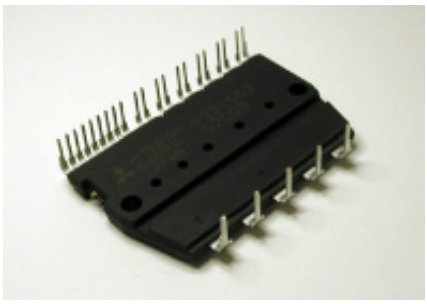
In the newly developed dual in-line package intelligent power module (DIP-IPM) Ver. 3 Series, the fifth-generation planar structure IGBTs or carrier stored trench-gate bipolar transistors (CSTBT) have been used to bring to market six new products with rated voltage of 600V and rated currents ranging from 5A to 50A. Direct driving by the 3V system MCU is now within range, making it possible to simplify the input interface.

Background

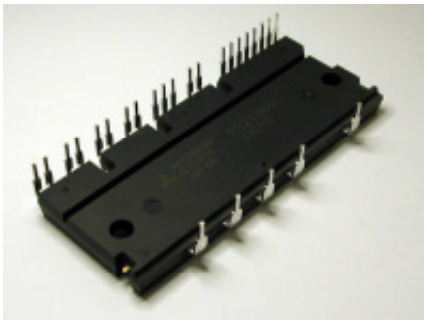
DIP-IPMs are intelligent power modules with a transfer mold structure, developed by Mitsubishi Electric Corporation for the home-appliance inverter market, and are used extensively in consumer white goods such as air conditioners, washing machines, and refrigerators. Although there has long been strong demand for smaller, more efficient, power modules with lower noise emission for the home-appliance inverter market, recently the stronger demand is for cost reduction, due to the recent decline in home electrical appliance prices.

Overview of the DIP-IPM Ver. 3 Series

Like the earlier DIP-IPM Ver. 2 series, the DIP-IPM Ver. 3 Series products are deployed in two types of packages, large and miniature, depending on the current ratings. Fig. 1 shows DIP-IPM Ver. 3 products, and Fig. 2 shows the structure within the package. The DIP-IPM Ver. 3 miniature package is manufactured from molded resin after mounting the power chip and the control IC on a frame, and has the exact same structure as the Ver. 2 miniature package. The DIP-IPM Ver. 2 large package is manufctured by performing resin molding after first mounting the power chip and the control IC on the frame (the first molding), and then performing resin molding again with an aluminum heat sink in place (the second molding). The DIP-IPM Ver. 3 large package is structured using only a single-step resin molding process after mounting the power chip and the control IC on the frame and after soldering separated copper heat sinks to the back of the frame of the power section. The use of this new package



(a) Miniature Package



(b) Large Package

Fig. 1 The DIP-IPM Ver. 3 packages

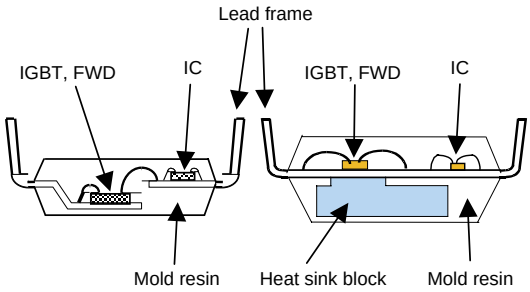


Fig. 2 Internal structures of the DIP-IPM Ver. 3 products

structure in the Ver. 3 large package makes it possible to reduce costs and to increase the capacity by increasing the efficiency of thermal dissipation. Table 1 shows a list of the DIP-IPM Ver. 3 Series product lineup.

As with the DIP-IPM Ver. 2, the internal circuitry in the Ver. 3 comprises a power circuit section (IGBTs and FWDs) with a three-phase inverter structure, and an LVIC and HVICs for

**Shinya Shirakawa and Touru Iwagami are with Power Device Works*

Table 1 List of DIP-IPM Ver. 3 Series Products

Product No.	Rating	Package
PS21562	5A/600V	Miniature
PS21563	10A/600V	
PS21564	15A/600V	
PS21865	20A/600V	Large
PS21867	30A/600V	
PS21869	50A/600V	

control. The LVIC provides IGBT gate-drive function, short-circuit protection, and control supply under-voltage protection, while the HVIC offers IGBT driver function and control supply under-voltage protection. Fig. 3 shows a block diagram of the inside of the DIP-IPM Ver. 3 (large package DIP-IPM).

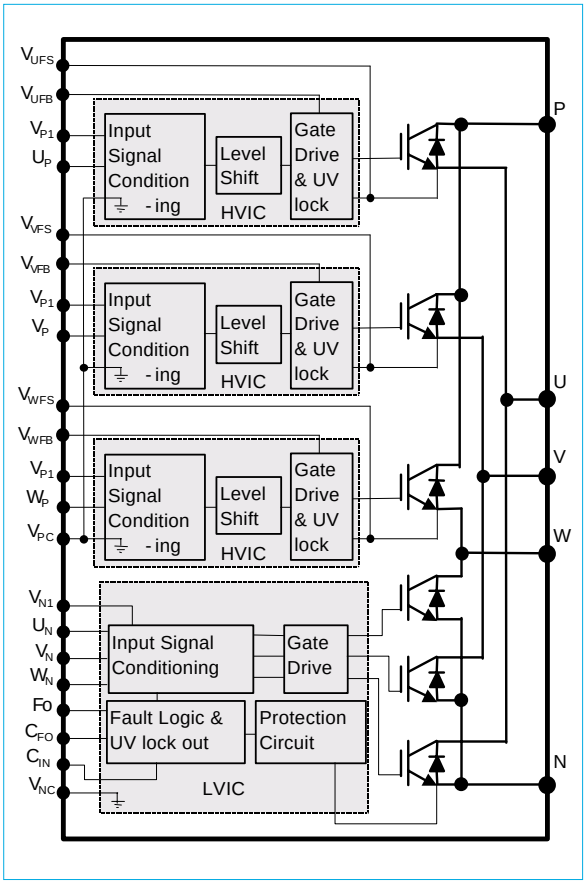


Fig. 3 Internal block diagram (large DIP-IPM Ver. 3)

Power-Device Technology

The DIP-IPM Ver. 3 Series uses fifth-generation planar IGBTs (0.6µm design rule) in all products with rated currents of up to 30A, and uses carrier stored trench-gate bipolar transistors (CSTBTs) in the product with the 50A rated current. This makes it possible to reduce the saturation voltage and shrink the chip size relative to the DIP-IPM Ver. 2, which is equipped with a fourth-generation planar IGBT.

The CSTBT, which has carrier-storage layer and a carrier concentration distribution nearly the same as that of a diode when in the ON state, is beginning to become practical as the next-generation power device, due to the advantage of enabling a saturation voltage even lower than that of conventional trench IGBTs.

ASIC Technologies

HVICs, where 24V CMOS elements and 600V withstand voltage DMOS elements are integrated on the same chip, are used as the high-side IGBT driver elements in the DIP-IPMs, making it possible for an MCU, etc., to drive the DIP-IPM directly, without the use of a opto-coupler. The use of a new process in the control IC has made it possible simultaneously to reduce the chip size and the circuit current. This, in turn, makes it possible to reduce the circuit current for the high-side IGBT gate drive so that the bootstrap capacitance can be reduced.

Packaging Technologies

A single-step molded structure with built-in separated copper heat sinks is used to increase the current capacity of the large-package DIP-IPM. The use of this new structure greatly increases the thermal dissipation capabilities over those of the conventional DIP-IPM Ver. 2 large packages.

Advantages

One advantage of the DIP-IPM Ver. 3 Series is its simpler input interface. Typically, MCUs are used to control DIP-IPMs, but in recent years the trend in MCU drive-supply voltages is shifting from 5V to 3V. The optimization of the input threshold values in the DIP-IPM Ver. 3 Series

for compatibility with 3V system input signals enables direct drive by 3V MCUs and digital-signal processors (DSPs). Furthermore, by using high-active I/O logic (where the output is high when the input is high) and integrating an internal pull-down resistor at the input of the DIP-IPM, the need to connect external resistors is eliminated, enabling simplified input-interface circuitry. Fig. 4 shows an example of a DIP-IPM Ver. 3 input interface circuit schematic in comparison with that of the DIP-IPM Ver. 2 (low active).

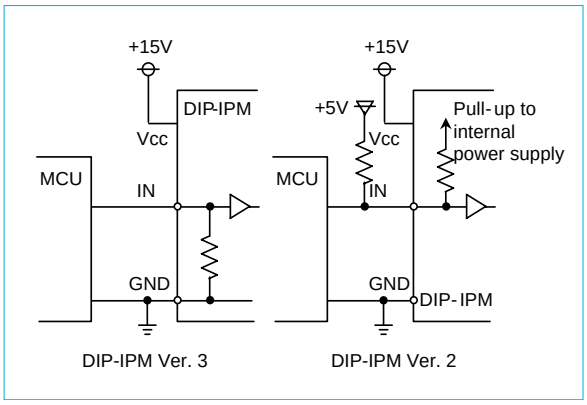


Fig. 4 Comparison of input interface circuits

The second advantage of the DIP-IPM Ver. 3 Series is the product lineup of large DIP-IPMs, with 30A and 50A rated current capacities. The use of the novel large packages with the high thermal dissipation and the low saturation voltage IGBTs (the fifth generation planar IGBTs and the CSTBTs) in the DIP-IPM Ver. 3 Series has enabled products with rated currents of 30A (PS21867) and 50A (PS21869). This makes it possible to use DIP-IPMs in motor-control applications with relatively large power capacitances that have, in the past, had to use conventional plastic case-type IPMs. This is a significant contribution to reduced system costs.

The third advantage of the new series is the product lineup of small DIP-IPMs with the rated current of 15A. Although the DIP-IPM Ver. 2 Series included products with rated currents from 3~10A in the miniature packages, the use of the fifth-generation planar IGBT in the DIP-IPM Ver. 3 Series has made it possible to add a 15A rated current miniature package product (PS21564). This in turn makes it possible to use the miniature-type DIP-IPMs in air-conditioner compressor applications, which is difficult for the DIP-IPM Ver. 2 miniature type.

Mitsubishi Electric Corporation will continue to supply DIP-IPM Series products fulfilling the needs of future markets as well as providing excellent cost/performance and excellent reliability based on a well-established market record. ❑

A New DIP-PFC Converter with Power-Factor Correction

*by Mamoru Seo and Xiaoming Kong**

Mitsubishi Electric Corporation has developed and marketed a new type of active converter dual in-line package power factor correction (DIP-PFC) that integrates a power-factor correction function with a current-rectification function for regulation of harmonic currents in inverter power supplies. In these products, not only is the package size smaller than the corporation's previous products as a result of the use of the transfer-mold technology, but this product has also reduced power losses through the use of a low-loss IGBT.

The Structure and Applications of DIP-PFCs

Fig. 1 shows the DIP-PFC developed by the corporation, and Fig. 2 shows its circuitry. The DIP-PFC is an all-silicon chip comprising only two low-loss IGBTs (Q1 and Q2), four high speed diodes (D1 to D4), and an IGBT driver (LVIC), sealed into a package fabricated through the use of the transfer-mold technique to form a compact power module.[1]

Fig. 1 A DIP-PFC

This circuit integrates the PFC function and the rectifying function, and is housed in a single small package fabricated using transfer-mold technology, while also contributing to reduced inverter system footprints and part counts by eliminating the external diode bridges which is necessary with conventional active-filter IPMs.

The DIP-PFC series includes two products with rated input currents of 15 and 20A(rms) for use in inverter applications up to the 3.7kW/200VAC class.

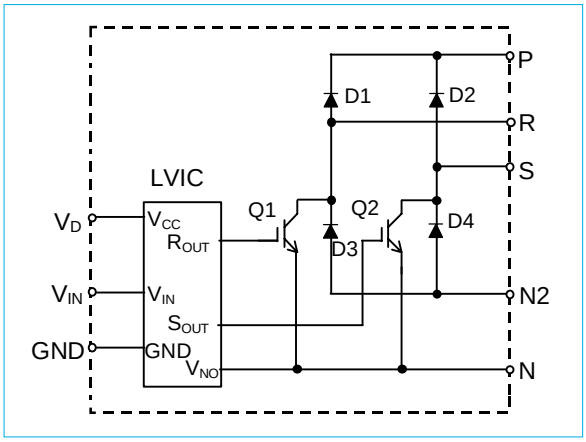


Fig. 2 DIP-PFC circuit configuration

Functions and Features of the DIP-PFC

DIP-PFC functions include:

* AC/DC current rectifying function:
  This converts a single-phase alternating current into a direct current using normal full-wave rectification.
* IGBT drive/protection functions:
  The LVIC equipped in the unit contains a drive circuit for two IGBTs and a control supply under-voltage lockout protection circuit.

The provision of an external power-factor correction control IC, which controls the switching of the IGBT, enables high performance full-switching PFC control and a variety of protection functions:[2]

1. The exclusion of the harmonic components of the input current makes it possible to achieve power factors of virtually 100%.
2. The output voltage feedback makes it possible to achieve a stabilized output voltage at the set value.
3. A variety of protection functions are available:
   Over-voltage repression at light loads (OV1).
   Output over-voltage protection (OV2)
   Short-circuit protection (SC)
   Soft-start function (SS)

**Mamoru Seo and Xiaoming Kong are with Power Device Works.*

Key Technologies

Problems that had to be overcome when developing the active converter using the transfer-mold method included thermal dissipation due to losses in the IGBT switching element and the control of surge voltages caused by the steep *dI/dt* when switching large currents rapidly. The following technologies were introduced to solve these problems.

A NEW CIRCUIT STRUCTURE. Circuits using the conventional single IGBT structure, shown in Fig. 3a have large per-IGBT losses because the current after full-wave rectification all goes into a single IGBT when the IGBT is turned on. On the other hand, in the dual-IGBT circuit that is currently used, shown in Fig. 3b, the current in one period goes through (1) and (2) in the figure, switching back and forth with each half wave, to two IGBTs, Q1 and Q2, matching the polarity of the AC power supply. This makes it possible to cut the current carrying period of each IGBT element in half, thereby cutting in half the power loss in each individual IGBT.

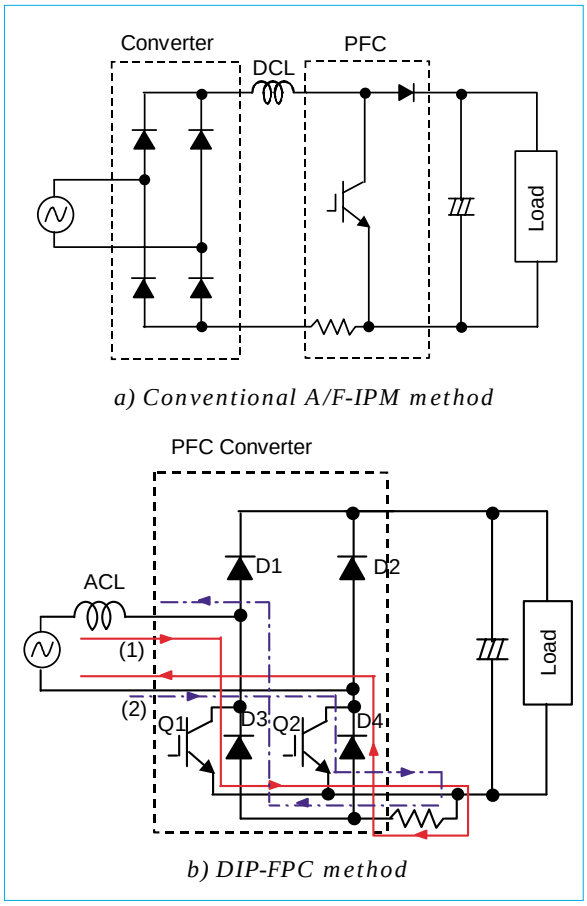


Fig. 3 Comparison of application circuits

OPTIMIZATION OF THE LEAD-FRAME PATTERN. The parasitic stray inductance of the pattern was minimized in order to reduce surge voltage when switching large currents rapidly.

DIP-PFC Specifications

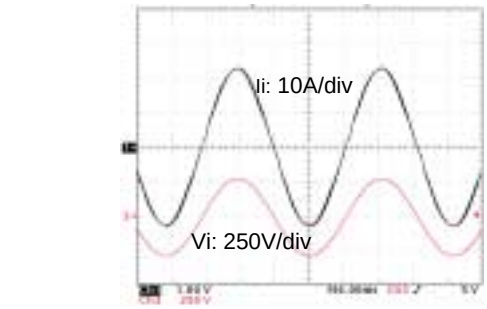
Table 1 shows the key specifications of the PS51259-A, a representative member of the DIP-PFC series. Fig. 4a shows the input current and input voltage waveforms when the PS51259-A is used with a resistive load. The input current is a sine wave, synchronized with the AC voltage, producing a power factor in excess of 99%. Harmonic current distributions such as shown in Fig. 4b now can be controlled to less than the current harmonic control level (i.e., IEC61000-3-2). Fig. 5 shows the results of loss simulations for the DIP-PFC (parameters used: V_I = 200V, V_0 = 380V, F_{SW} = 20kHz). The DIP-PFC reducted losses by approximately 10% below the total losses when the conventional active filter IPM-PM52AUVW060 is used with an external diode bridge.

Application of the DIP-PFC

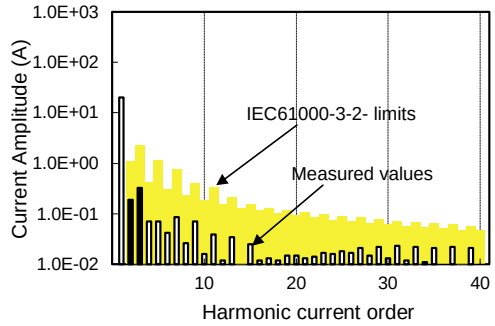
A specific control IC, developed in parallel with the DIP-PFC, has to be used in conjunction with it for proper operation. The DIP-PFC is designed with the same external dimensions as the corporation's large DIP-IPM, even using the same mounting height, and so can use the same heat

Table 1 Key Specifications of a DIP-PFC (PS51259-A)

Item	Symbol	Parameter	Rated Value
Input power-supply voltage	Vi	Between S-R terminals	90~264V
Output voltage	Vo	Between P-N terminals	450V (max)
Input current (rated)	Ii	V_I = 200V, V_O = 300V, f_{PWM} = 20kHz, $T_C \leq 90°C$	20A (rms)
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_D = 15V, V_{IN} = 5V, Ic = 50A	1.8V (typ)
Diode forward voltage drop	V_F	I_F = 50A	2.1V (typ)
Switching time	Ton	Vcc = 300V, V_D = 15V,	0.29µs (typ)
	Toff	I_C = 30A, T_J = 125°C	0.46µs (typ)
	Trr	V_{IN} = 5⇔0V, inductive load	0.13µs (typ)
Diode peak recovery current	Irr	Vcc = 300V, V_D = 15V, I_C = 30A, T_J = 25°C	13A (typ)



a) Input current and voltage waveforms



b) Harmonic current measurement results

Fig. 4 Input current waveform and harmonic distribution

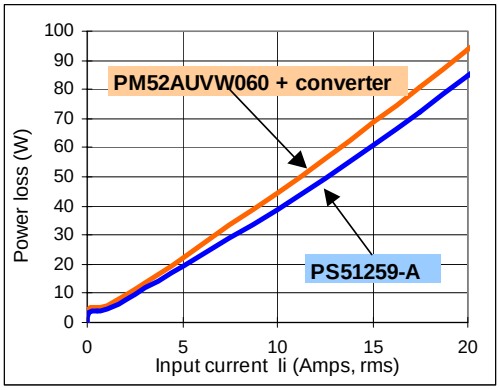


Fig. 5 Comparison of power losses between the DIP-PFC and the A/F-IPM method

sink when used paired with the DIP-IPM. This makes it possible to minimize the length of the interconnect patterns and the size of the printed circuit boards, thereby reducing system cost.

Fig. 6 is a photograph of the DIP-PFC inverter unit produced by the corporation for air-conditioner compressor control consisting of a small control circuit board with the control IC and the DIP-IPM mounted together with the DIP-PFC.

With growing market demand for further improvements in efficiency and reduced costs, it is our hope to produce products with even higher performance and more added value in the future. ❑

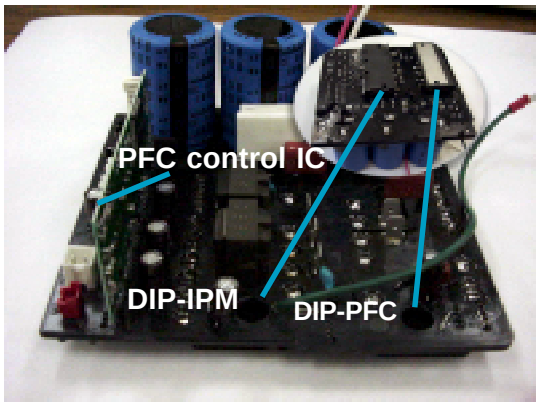


Fig. 6 Air-conditioner inverter control board with PFC

References

[1] J. Domlon, J. Achhammer, J. Iwamoto, M. Iwasaki, "Power Modules for Appliance Motor Control," IEEE Industry Applications Magazine, July 2002, Vol. 8, No. 4, pp 26 - 34.

[2] M. Iwasaki, et. al., "An Integrated Power Factor Correction Module With Dual In-line Package," Proceedings of PCIM 2003, Germany, pp189 - 193.

6.5kV IGBTs

*by Eisuke Suekawa and Yasuto Kawaguchi**

Recently there has been a shift from the conventional GTO thrystors to high-voltage IGBT (HVIGBT) modules as power-switching devices in converters and inverters in response to market needs for smaller, lighter, and quieter systems in sectors that use large electric motors such as trains, electric power, and heavy industry.

Mitsubishi Electric Corporation has already marketed a 4.5kV-class HVIGBT capable of controlling 3.0kV line voltages in railroad applications and other industrial applications, but there are calls for the development of IGBTs with even higher withstand voltages that can control line voltages up to 4.3kV. In response to these demands, the corporation has developed a 6.5kV-class IGBT chip using a light punch through (LPT) structure to optimize the cell structure to provide an improved reverse-bias safe-operation area (RBSOA) and short-circuit safe operation area (SCSOA) capabilities without sacrificing critical electrical characteristics.

The Chip Design Concept

IGBT structures can be categorized into punch through (PT) types and non-punch through (NPT) types. Because the PT types have an n^+ buffer layer, the n^- base layer can be made thinner, which is useful in reducing the collector-emitter saturation voltage ($V_{CE(sat)}$) and the turn-OFF loss (Eoff). However, in IGBTs with rating voltages in excess of 1.7kV, if the n^- base layer is too thin, the increase in the h_{FE} of the internal pnp transistors will cause an increased leakage current, restricting the RBSOA. To solve these problems, the new 6.5kV-class IGBT uses an LPT structure in which the thickness of the n^- base layer (tn^-), the specific resistivity (ρn^-) and the collector structure have been optimized.

Fig. 1 shows cross-sectional schematic diagrams of a conventional NPT-IGBT and an LPT-IGBT. In the LPT-IGBT, the wafer design is performed using the tn^- and the ρn^- so that the depletion layer does not reach the n^+ buffer layer when the supply voltage applied is within the actual use range, and so that the depletion layer reaches the n^+ buffer layer when the rated voltage is applied, thus making it possible to choose the minimal tn^- that is able to insure the required collector-emitter breakdown voltage characteristics (V_{CES}). Consequently, the LPT-IGBT makes it possible to reduce the $V_{CE(sat)}$ and the Eoff.

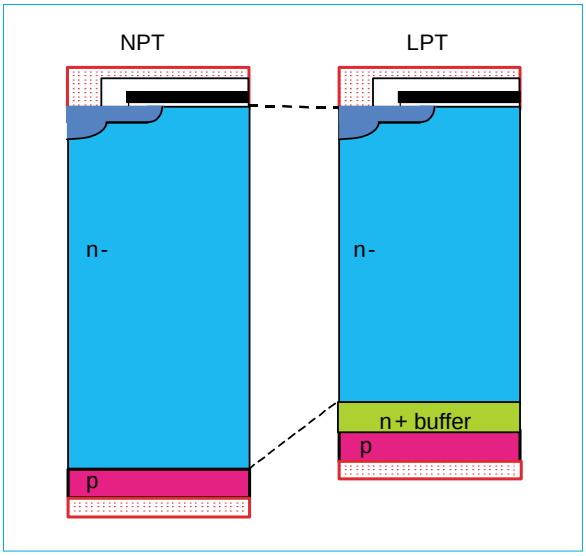


Fig. 1 Comparison of conventional NPT and LPT chips

Generally, in railroad applications, the rated withstand voltage must be guaranteed for junction temperatures Tj between –40°C and +125°C. Fig. 2 shows the V_{CES} as a function of the tn^-

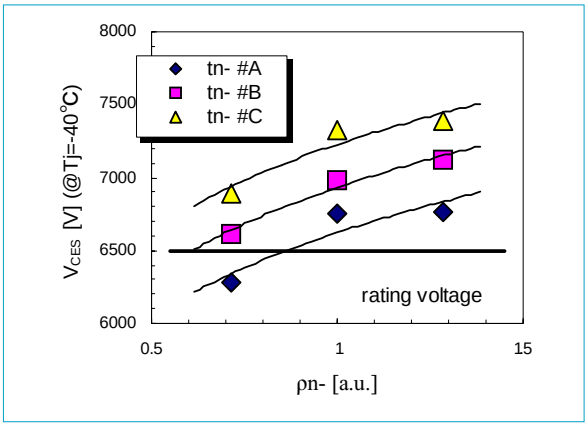


Fig. 2 Dependence of breakdown voltage on ρn^- and tn^- (at Tj = –40°C)

**Eisuke Suekawa is with Power Device Works and Yasuto Kawaguchi is with Fukuryo Semicon Engineering Corporation.*

and the ρn⁻ parameters at Tj = –40°C. The V_{CES} has a positive temperature dependency, and the lower Tj, the lower the V_{CES}. From the figure, it is clear that the selection of the specification A wafer n⁻ layer makes it possible to guarantee the rated voltage V_{CES} in the range of operating temperatures required for railroad applications.

Reduced Leakage Current

The IGBT leakage current (I_{CES})is similar to the collector-emitter reverse current (I_{CE}) of a pnp transistor at the open-base condition obtaining in an IGBT. From transistor theory, the following equation is obtained:

$$I_{CEO} = h_{FE}\,(pnp) \times I_{CBO} \quad \text{..... Eq. 1}$$

where I_{CBO} is the collector-base reverse current and h_{FE} (pnp) is the common emitter current gain.

Eq. 1 indicates that the h_{FE} (pnp) of the internal pnp transistors should be small in order to suppress their I_{CBO}, but low h_{FE}(pnp) causes $V_{CE(sat)}$ to increase. Fig. 3 shows the dependence of I_{CES} and $V_{CE(sat)}$ on the ratio between the p⁺ collector-layer concentration and the n⁺ buffer-layer concentration (γ_1) at high temperatures. Here, it is evident that at high temperatures the I_{CES} can be suppressed and spikes in the $V_{CE(sat)}$ can be prevented by having a γ_1 of about 10.

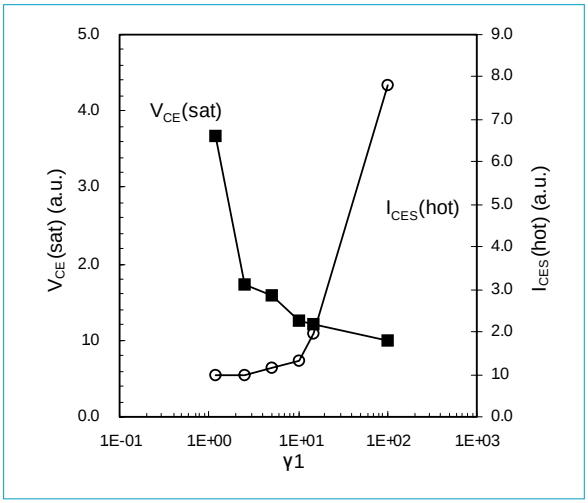


Fig. 3 Dependence of $V_{CE(sat)}$ and hot-collector leakage current ($I_{CES(hot)}$) on the p⁺ collector-layer/n⁺ buffer-layer concentration ratio (γ_1)

Improvement of RBSOA

When the IGBT turns OFF, the holes that exist in the n⁻ layer pass through the p base layer to be discharged into the emitter electrode. At this time, the hole current that is discharged forms the base current of the npn transistors in the IGBT. Fig. 4 shows schematically the hole-current path in the conventional IGBT cell structure. When the resistance of the p base layer directly under the n⁺ source layer (the pinch resistance) is high, the effects of the voltage at this part cause the npn transistor to turn ON, preventing the thyristor effect from being controlled by the gate, resulting in thermal breakdown in the IGBT. Reducing the pinch resistance is effective in increasing the amount of current that can be controlled when the IGBT turns OFF, so pinch resistance was optimized in this experiment.

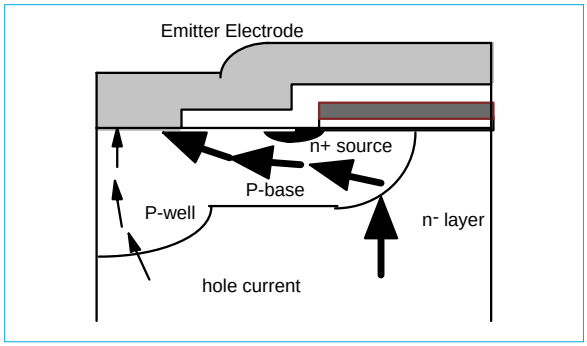


Fig. 4 Path of hole current in the conventional cell structure

Fig. 5 shows the controllable current when switching OFF as a function of the pinch resistance. The figure shows that even a reduction in pinch resistance of about 40% does not improve the amount of controllable current when switching OFF.

Next, investigations were performed into increasing the electric field in the p well layer by increasing the diffusion depth of this layer in order to reduce the hole current extracted through the p base layer directly under the n⁺ source layer. Fig. 6 shows schematically the path followed by the hole current in a cell structure with a deeper p-well layer. In the experiments, chips were manufactured on a trial basis with increases of about 5% and about 9% in the dif-

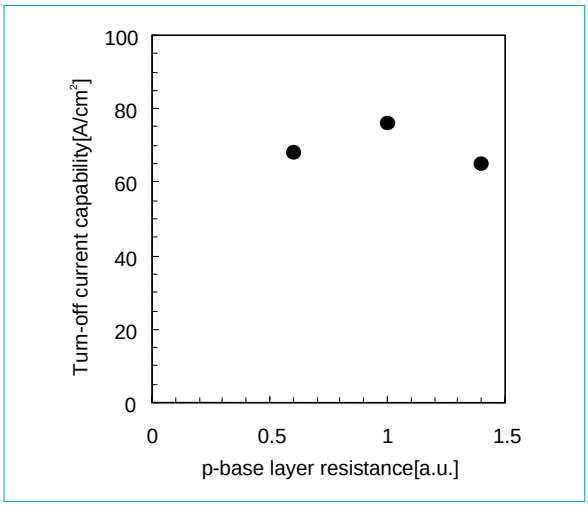


Fig. 5 Dependence of turn-OFF current capability on p-base layer resistance

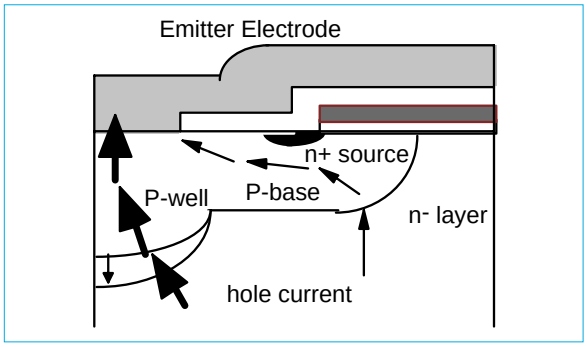


Fig. 6 Path of hole current in a cell structure with a deeper p-body layer

fusion depth of the p- well layer compared with conventional IGBTs. The results, as shown in Fig. 7, indicate that the controllable current

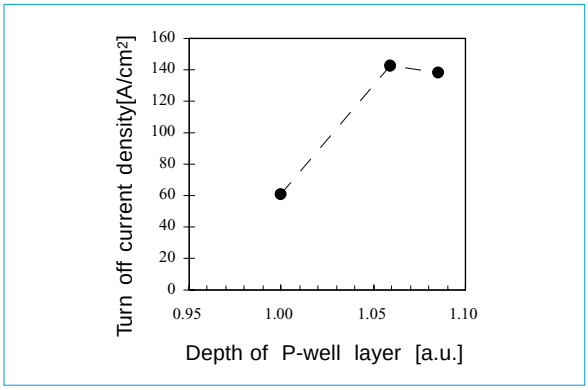


Fig. 7 Dependence of turn-OFF current capability on depth of p well layer

when switching OFF improved by a factor of some two- or three-fold over the conventional IGBT. These results suggest that the parasitic behavior of the npn transistors within the IGBT can be suppressed by reducing the resistance of the p-well layer and by transferring the concentration of the electric field from the p-base layer to the p-well layer. In addition, optimizing the design of the p-well layer more than doubled the controllable current at switch OFF compared with the conventional design, without impairing major electrical characteristics such as $V_{CE(sat)}$, Eoff, and V_{CES}.

Chip Characteristics

Trial manufacturing was also performed for chips rated at 6.5kV/33A. These chips were designed with a rated current density of 35A/cm². Fig. 8

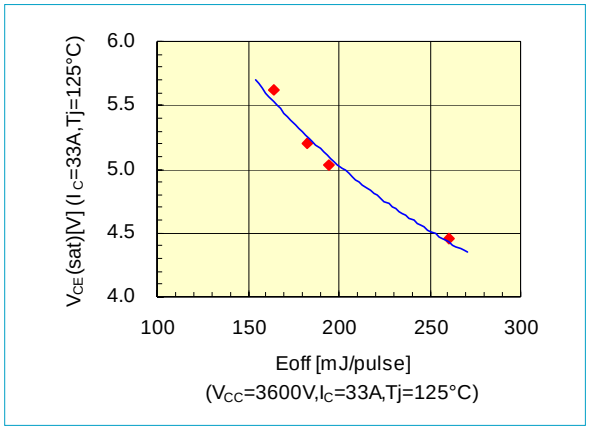


Fig. 8 Trade-off relationship between $V_{CE(sat)}$ and Eoff

shows the trade-off characteristics between $V_{CE(sat)}$ and Eoff, and Fig. 9 shows the dependence of Eoff on V_{CC}. The use of the LPT structure, in which the wafer n⁻ layer has been optimized, prevented any large increases in Eoff given the power-supply conditions found in actual use situations.

Fig. 10 shows the waveforms for evaluating the RBSOA with V_{CC} = 4.3kV, J_C = 143A/cm² and Tj = 125°C. The optimization of the cell structure enables turnoff of approximately four times the rated current density.

Fig. 11 shows the waveform for evaluating the short-circuit capabilities. We confirmed that there are no breakdowns for ON pulse widths

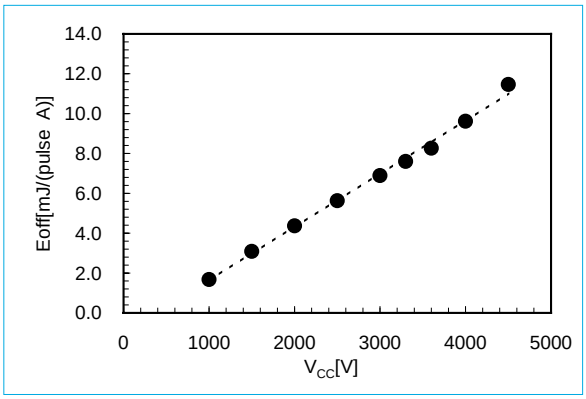


Fig. 9 Dependence of Eoff on V_{CC}

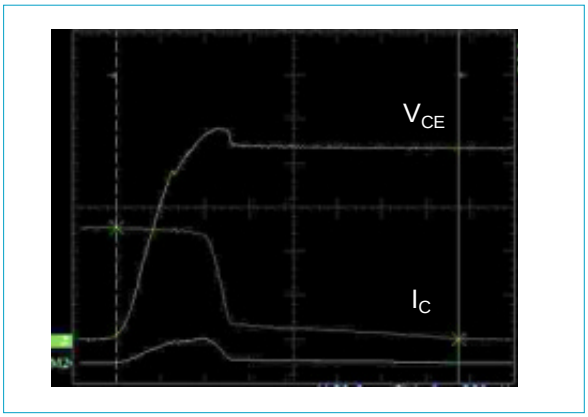


Fig. 10 RBSOA waveforms (V_{CC} = 4.3kV, I_C = 134A, Tj = 125°C) (V_{CE}: 1kV/div, I_C: 50A/div, Time: 1µsec/div)

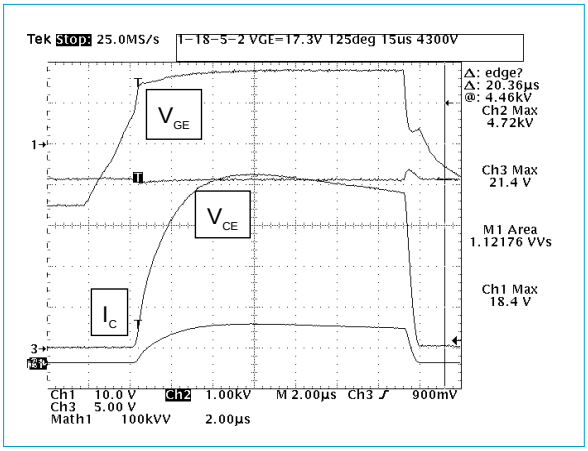


Fig. 11 SCSOA waveforms (V_{CC} = 4.3kV, Tj =125°C) (V_{CE}: 1kV/div, V_{GE}: 10V/div, I_C: 50A/div, Time: 2µsec/div)

(tw) of up to 13µsec under the conditions of V_{CC} = 4.3kV and Tj = 125°C.

This project confirmed that the newly developed 6.5kV-class IGBT possesses the RBSOA characteristics and short-circuit capabilities required by the market, with no penalties in terms of other major electrical characteristics. Work is currently underway on HVIGBT modules containing these 6.5kV-class IGBT chips, which are not only expected to find applications in a broad range of fields but are also to contribute greatly to the miniaturization of power units. ❑

2kV Breakdown Voltage SiC-MOSFET Technology

*by Masayuki Imaizumi and Yoichiro Tarui**

Mitsubishi Electric Corporation has fabricated a high-voltage power MOSFET using silicon carbide, which is looked upon as the most likely semiconductor for the next generation of power devices. The use of an epitaxial layer in the channel part provides improved conductivity, producing an on-resistance of 40mΩ·cm^2 for a breakdown voltage of 1.9kV. This value corresponds to 1/25 of the theoretical limit for silicon unipolar devices.

Characteristics of the Epitaxial Layer MOS Channel

Silicon carbide (SiC) is the leading candidate to become the semiconductor material for next-generation power devices due to its physical properties, which are superior to silicon (Si). Because unipolar devices are able to take advantage of the benefits of SiC, many research organizations are working on developing metal-oxide-semiconductor field-effect transistors (MOSFETs) using this material.[1-4] However, the conductivities obtained in SiC-MOSFETs are nowhere near those predicted by theoretical models. The biggest reason for the difference is that the conductivity in the MOS channel is low (i.e., the effective mobility in the channel is low). This is a result of the high density of electron traps in the SiC MOS interface, which results in the capture of channel electrons and in increased Coulomb scattering due to these captured electrons. The corporation has improved the MOS channel conductivity by the use of a high-quality n-type epitaxial growth layer in the channel.[5]

The corporation has performed systematic investigations into the effects of the doping concentrations and thickness of the channel epi-layer on conductivity characteristics in SiC-MOS channels, leading to the discovery that the field-effect mobility exhibits different gate-voltage dependency characteristics when there is a drain current and the gate voltage is near to 0V (i.e., when there is a so-called "buried channel") from the dependency observed when the carriers are concentrated at the interface alone. Fig. 1 shows a cross-sectional diagram of a vertical MOSFET fabricated for evaluating the mobility

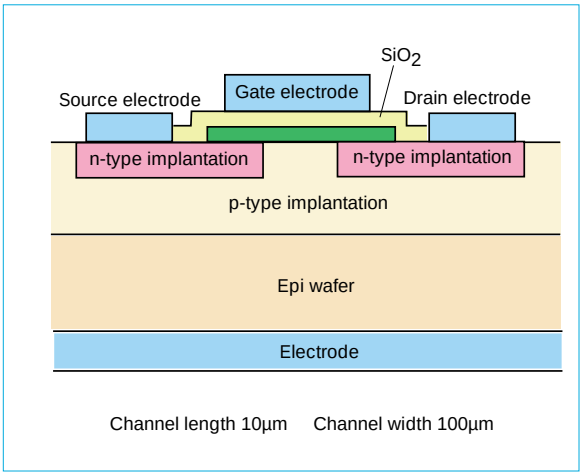


Fig. 1 Cross-sectional view of MOSFET for mobility evaluation

in the epi-layer channel, and Fig. 2 shows typical corresponding I_D-V_G characteristics. The buried-layer channel-type characteristics produced a peak value of about 60cm^2/Vs for the field-effect mobility. When the gate voltage was increased, the mobility fell with the increasing density of carriers concentrated at the MOS interface, dropping to a value of about 7cm^2/Vs. This indicates that high mobilities are produced when the effects of the MOS interface are small in the buried channel (which has diffuse boundaries) while the gate voltage is low, but when the carriers begin to concentrate at the inter-

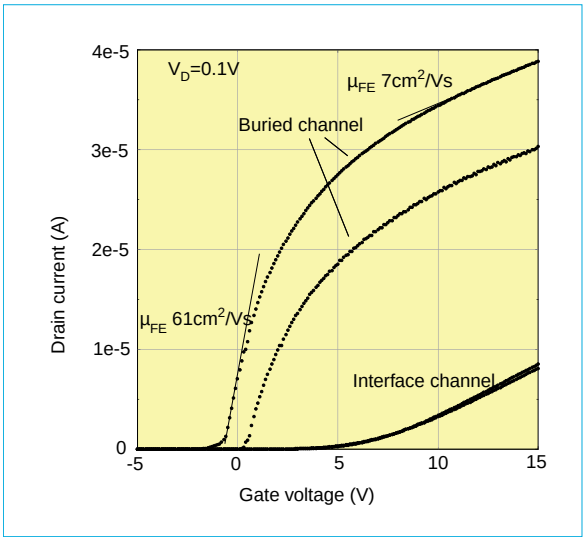


Fig. 2 I_D - V_G characteristics of planar MOSFETs

**Masayuki Imaizumi and Yoichiro Tarui are with the Advanced Technology R&D Center*

face, the mobility falls because of the effects of the charge traps. On the other hand, for an interface accumulation channel, the dependence of the field-effect mobility on the gate voltage is low when the channel-layer thickness and doping concentrations have been optimized, producing a value of about 7cm^2/Vs. Although the asymptotic value for the mobility in a buried channel is near to the mobility in the interface accumulation-type channel, this is because the quality of the MOS interface determines the value for the mobility. In an inversion MOS channel lacking a channel epi-layer over the p-type implanted layer (fabricated for comparison), the field-effect mobility was extremely low, with a value below 1cm^2/Vs. The conductivity achieved through the use of the n-type epitaxial layer in the MOS channel is clearly an improvement over this low mobility. In the future, these characteristics will be improved through further research including oxide-layer fabrication methods.

The improvement in conductivity when a buried channel is formed is large. However, when there is a buried channel, the OFF characteristics when the gate voltage is 0V can be problematic (i.e., the ON/OFF ratio is low). Because of this, the channel epi-layer fabrication conditions must be selected according to the characteristics required of the MOSFET. In the high-voltage MOSFETs described below, the goal is to obtain a normally-OFF status, and so the channel epi-layer was fabricated using conditions that do not cause the formation of a buried channel layer.

The High-Voltage MOSFET Structure and Fabrication Method

Fig. 3 shows a cross section of the structure of the high-voltage MOSFET produced in this project, and Fig. 4 is a photomicrograph of the completed electrode pattern. The gate and source electrodes are interlaced, and the drain electrode is fabricated on the back surface. The channel length is 2µm, and the channel widths totaled 7.56mm (270µm x 28). A junction termination extension (JTE) 100µm wide was provided enclosing the device, with the electric field terminated at the surface. The devices, including the JTE regions, were approximately 800×800µm, and the active area of each MOSFET was 270 × 420µm. Although the MOSFETs fabricated in this project were small, in the future it will be possible to increase the area of the MOSFETs by improving the quality of the SiC substrate.

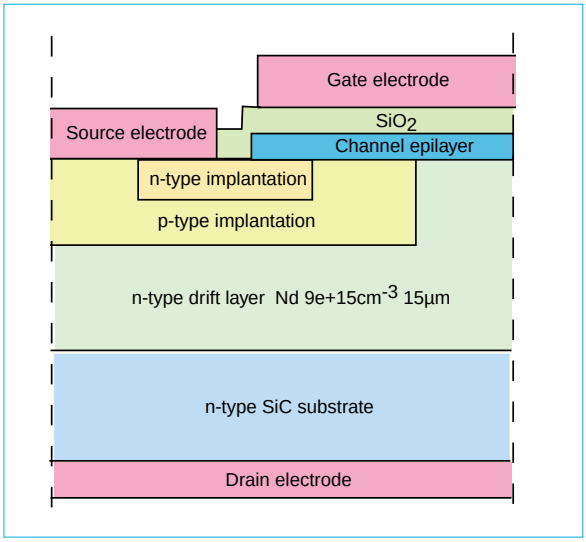


Fig. 3 Cross-sectional view of vertical MOSFETs

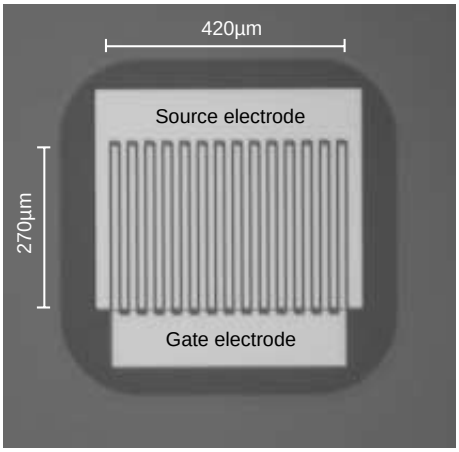


Fig. 4 Top view of vertical MOSFET

A summary of the MOSFET fabrication process follows. An n-type 4H-SiC was used as the substrate, and an epitaxial process was used to fabricate a drift layer 15µm thick, with a donor concentration of 9×10^{15}cm^{-3}. Aluminum was implanted as a p-type dopant into the well region and the JTE regions, and N ions were implanted into the source region as an n-type dopant, after which activation annealing was performed in an Ar ambience for 30 minutes at 1,600°C. Because activation annealing after ion implantation in SiC requires high temperatures, there are still problems to be solved, such as those of surface roughness and various equipment issues. The epitaxial growth for the channel layer was performed after the activation annealing. The channel epi-layer in this project was 0.2µm thick, with a donor concentration of 1×10^{17}cm^{-3}, and was of the interface accumulation type, as shown in Fig. 2. Although activation annealing in SiC typically ruins the planarity by producing

bunched giant steps on the surface of the SiC, the planarity of the surface was greatly improved through the growth of the channel epi-layer.[5] After the growth of the channel epi-layer, reactive-ion etching (RIE) was used to remove the unneeded parts of the channel epitaxial layer, and, after a sacrificial oxide process, the gate-oxide layer was fabricated. The gate oxide was grown by a thermal-oxidation in a pyrogenic wet-ox (steam/oxygen) ambience, performed at 1,100°C for two hours. Aluminum was used for all of the electrodes, fabricated using electron-beam evaporation with lift-off patterning.

Evaluation of Electrical Characteristics

Fig. 5 shows an example of the I_D -V_D characteristics of the MOSFETs produced. Although the threshold voltage was high, at about 10V, excellent normally-OFF properties were obtained. With a gate voltage of 25V, the ON resistance was 40mΩ·cm^2. A breakdown voltage of 1.9kV was obtained with a gate voltage of 0V. This breakdown voltage value is about the same as the theoretical breakdown voltage for a pn junction calculated based on the donor concentration in the drift layer, indicating that the JTE and other elements had been formed in accordance with the design. As evident from Fig. 6, the value for the ON resistance relative to the SiC-MOSFET breakdown voltage is about 1/25th that of the theoretical limit value for a silicon unipolar device, vastly superior to the characteristics of an Si-MOSFET. However, the value was still far from the theoretical value (1~2mΩ·cm^2) for SiC.

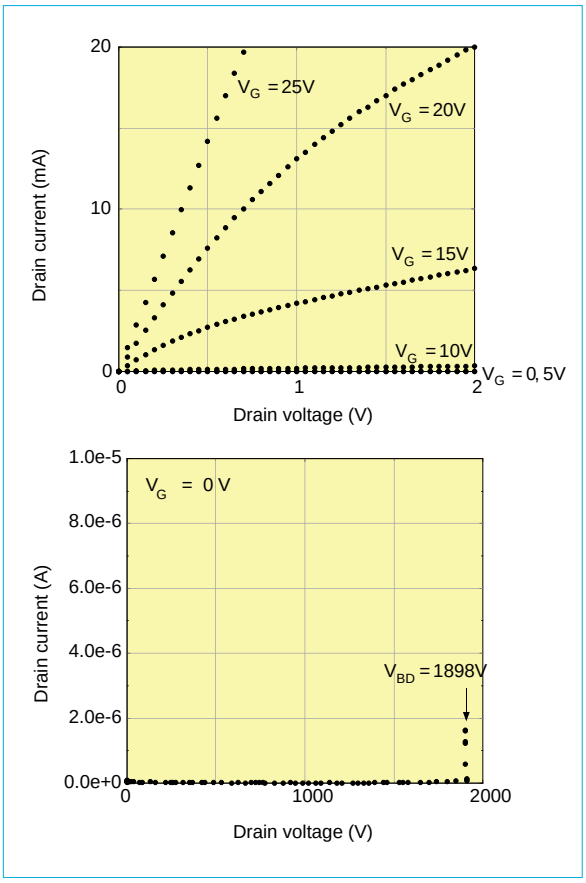


Fig. 5 I_D - V_D characteristics of vertical MOSFETs

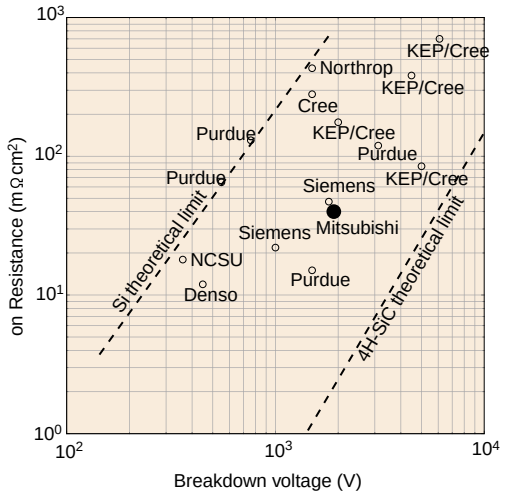


Fig. 6 Relationships between ON resistances and breakdown voltages

When the resistance value is measured for the comparative sample of a MOSFET with the same structure but with n^+ doping in the channel part, a value of 20mΩ·cm^2 was obtained for the active region. This value is thought to indicate the resistance excluding the resistance of the MOSFET channel part, suggesting a value of 20mΩ·cm^2 was obtained for the channel resistance. Because this high value for the channel resistance is due to low channel mobility, it is necessary to improve the present 5~10cm^2/Vs mobility to 50cm^2/Vs or more. When it comes to the resistance of the other parts of the devices outside the channels, these can be reduced substantially by optimizing the process and structure, and we anticipate that these improvements will follow through steady technological advances. ❑

References

[1] S. Ryu, A. Agarwall, J. Richmond, J. Palmour, N. Saks and J. Williams: IEEE, Electron Device Letters, 23, 321 (2002).

[2] R. Schorner, P. Friedrics, D. Peters and D. Stephani: Applied Physics Letters, 80, 4253 (2002).

[3] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwall and J. H. Palmour: IEEE, Electron Device Letters, 49, 658 (2002).

[4] R. Kumar, J. Kozima and T. Yamamoto: Japanese Journal of Applied Physics, 39, 2001 (2000).

[5] M. Imaizumi, J. Tanimura, Y. Tarui, H. Sugimoto, K. Ohtsuka, T. Takami and T. Ozeki: Journal of Crystal Growth, 237-239, 1219 (2002).

New Power-Element Technology

*by Tadaharu Minato and Hideki Takahashi**

Improvements in wafer processing technologies such as miniaturization and thin-wafer technology have improved the performance of our power semiconductors. Just as DRAMs drove LSI technology, low-voltage trench-gate MOSFETs, useful in miniaturization, are the wafer-process technology drivers in power semiconductor devices, with the technologies advancing from the half-micron domain to the quarter-micron domain. In power semiconductor devices, which are basically discrete elements with electrodes on both the front and back sides of the wafer, the key technologies are thin-wafer technologies such as light punch-through-type carrier-stored trench-gated bipolar transistors (LPT-CSTBTs). This thin wafer technology not only improves the cost/performance ratio in IGBTs but can also supplement the conventional functionality of IGBTs by those of reverse blocking-types (RB-IGBTs) and reverse conducting-types (RC-IGBTs).

In power semiconductor devices there is a trade-off between the forward current conducting capabilities (the ON resistance and/or the forward voltage drop) and the turn-off capabilities (the forward-blocking capabilities), where advances in these devices are measured in terms of improvements in this trade-off relationship. For bipolar IGBT devices, forward voltage drop *vs.* turn-off loss is the performance metric for the trade-off relationship, while the corresponding trade-off metric for unipolar MOSFET devices is specific ON resistance *vs.* forward blocking voltage. Of course, of greater importance than any other characteristics is that the device does not fail, or in other words, that the safe operation area (SOA) whether for forward-bias (FBSOA), reverse-bias (RBSOA), or short-circuit (SCSOA), is adequately wide given the application. Consequently, power semiconductor devices are actually not evaluated in terms of only the trade-off between the simple ON characteristics and OFF characteristics, but rather, as shown on the left of Fig. 1, performance is determined in a triangular trade-off relationship that includes these three different safe operation areas. As shown on the right-hand side of Fig. 1, these relationships comprise lower-level trade-off relationships.

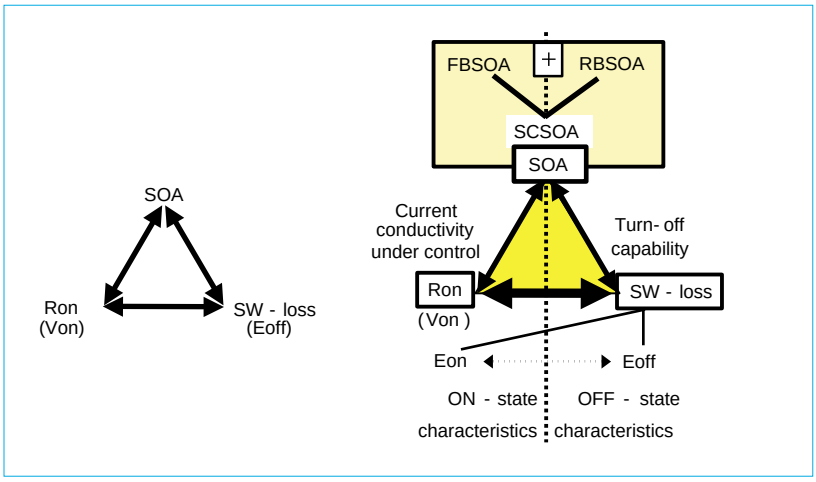


Fig. 1 The triangular trade-off (left), shown in detail (right)

Given the above, it is best for the materials from which the devices are made to have superior physical properties, and it can be anticipated that in the coming years, silicon devices will be supplanted by SiC devices and diamond devices. The efforts of Mitsubishi Electric Corporation in this area are described in a separate paper.

MOSFETs As Technology Drivers

In low-voltage MOSFETs (of the 100V class and below), the channel resistance (Rch), which is determined by the MOS gate structure, and the charge accumulation layer resistance (Racc) are the dominant factors in the total ON resistance of MOSFETs. These resistances account for more than 80% of the total resistance in 20-volt class devices. The implication is that shrinking the unit cell size and increasing the channel density of the microscopic processes is extremely effective in decreasing the ON resistance. In the year 2000, the corporation developed its sixth-generation pseudo-0.35μm trench MOSFET,[1] and then in 2003, the corporation developed a trench MOSFET (SAT-MOS) with an ON resistance of 0.7mΩ·cm^2, using

**Tadaharu Minato and Hideki Takahashi are with Power Device Works.*

the 0.35µm VLSI wafer processing technology and its self-alignment contact (SAC) trench technology.[2]

On the other hand, in the medium- and high-voltage classes, where the resistance is dominated by that of the N⁻ drift layer (the thickness and doping concentration of which define the forward-blocking voltage), the corporation developed the super-trench power MOSFET (STM) [3-4] applying its own proprietary trench technology. The "Si limit," which is the primary physical constraint in the trade-off between the forward blocking voltage and the specific ON resistance in unipolar devices, has been broken by using the multi-reduced-surface field (multi-RESURF) effects, so that a 300 volt-class STM with a planar gate made a breakthrough in ultralow specific ON resistance only 60% of the silicon limit. As shown on the right-hand side of Fig. 2, the multi-RESURF effect is obtained by a structure of repeated microscopically alternating p-type and n-type columns.

In STM, the repeated p-type and n-type layers are formed using the corporation's proprietary structure in which boron and phosphorus ions are implanted diagonally into the left and right side walls of a deep groove (trench). When compared to the multi-layer epitaxial method, used to produce similar effects in other companies, the use of this method makes it possible to simplify the manufacturing processes, using structures and processes that are well-suited for miniaturization. However, there is an extremely strong trade-off relationship between the specific ON resistance and the avalanche SOA, so STM devices have been more difficult to use than conventional devices (whether MOSFETs or IGBTs).

In the middle- and high-voltage domains, where SOA (the metric which expresses the specific ON resistance to the avalanche condition capability) is more important than the ON resistance, optimizing the conventional planar gate-type MOSFET (or planar MOS) is as effective as ever. The corporation's highly avalanche-resistant planar MOS-FET, as shown in Fig. 2, successfully produces the lowest ON resistance characteristics (140% of the silicon limit) of all conventional non-multi-RESURF structures.

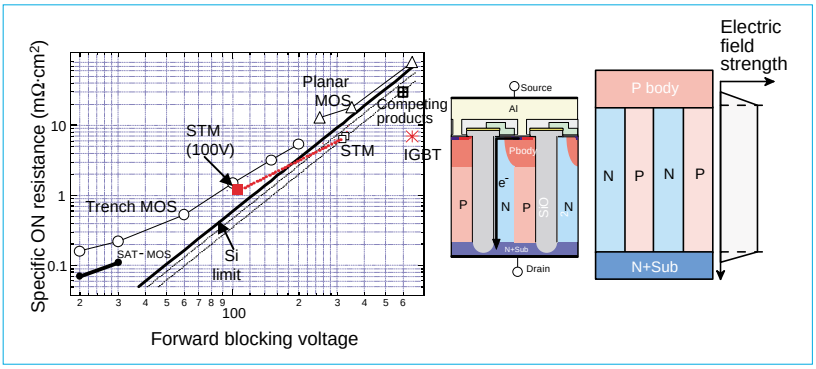


Fig. 2 The relationship between the forward blocking voltages and specific ON resistances in various MOSFETs

Evolution of IGBTs

As with MOSFETs, the performance of IGBTs has also advanced in parallel with those in wafer processing, such as increasing miniaturization. The corporation has succeeded in reducing forward voltage drops by applying the trench structure to the MOS gates of power semiconudctor devices instead of the device isolation used in large-scale integrated circuits[5,6]. In trench-gate structures, it has become possible to increase the level of integration in terms of both processing technologies and device operation, without increasing the forward voltage drops due to the JFET effect that is such an impediment to further miniaturization in planar gate structures. However, there is a problem in reducing the forward voltage drop by increasing the level of integration. This is the fact that it can lead to an increase in the peak collector current (I_{cp}) when the resistive and/or inductive load is shorted, making it difficult to maintain the SCSOA.

The product SOA is realized by the provision of a real-time current control (RTC) circuit and by the use of an intelligent power module (IPM), in addition to innovations in the cell structure such as adjusting the emitter-ballast resistance. From the perspective of increasing the strength of the individual components while further reducing costs, the SCSOA has been increased by sacrificing the minimum forward voltage drop through the adoption of a wide cell-pitch structure to keep the saturation current relatively low, relaxing the cell pitch rather than making it dense with trench gates.

CSTBTs. In addition to adopting a trenched-gate structure, in the carrier-stored trench-gate bipolar transistor (CSTBT) shown in Fig. 3, an n-type layer with a higher concentration than the n⁻ drift layer, termed the carrier accumulation layer, was fabricated in order to reduce the forward voltage drop[7]. The electrons, n-type carriers injected from the channel of the trenched gate MOS gate, spread easily into the CS layer, which has a higher concentration than the n- drift layer, making it easy to adjust the resistivity. At the same time, it is more difficult for the holes that are injected from the p-type collector layer on the

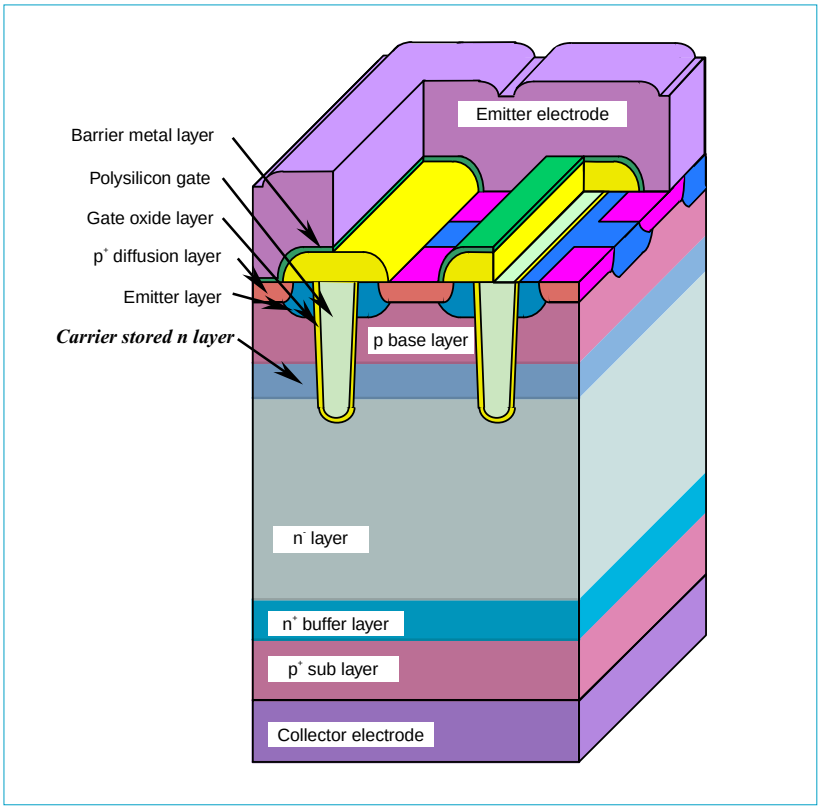


Fig. 3 The CSTBT structure

back surface to enter into the p base layer, because this enlarged energy barrier of the PN junction is the result of a junction between the high concentration n-type CS layer and the p base is higher than that of the junction between the relatively low concentration n– drift layer and the p base. The result is that the conditions for charge neutralization are fulfilled directly under the p base, causing a larger carrier accumulation effect, and thus reducing the forward voltage drop. Note that the principal of the CS layer can be applied to planar-gate structures as well.

LPT DEVICES. In parallel with the improvements in IGBT cell structures, the corporation has also created an LPT-type device using thin-wafer technologies. As a shown in Fig. 4, IGBTs have been ascending an evolutionary spiral from the non-punch-through (NPT) type to the punch-through (PT) type using dual-stage epitaxial crystal growth, and through the thin wafer NPT type, to the light-punch-through (LPT) type (Fig. 5), which is an advanced PT-type thin water.

The LPT structure resulted from the goal of improving cost performance, but is also extremely valuable because of the increased flexibility in device design. In the LPT structure the p collector can be fabricated with a relatively low concentration and thus has positive concentration characteristics that are desirable from the point of view of SOA, enabling unipolar MOS-FET-type output characteristics.

NEW FUNCTIONAL DEVICES. Although the new functional devices have textbook structures and principles, they have been difficult in terms of manufacturing technology. Now, however, thin-wafer technology has enabled their development, so not only have the reverse-blocking IGBTs (RB-IGBTs) described in another article in this volume achieved sufficient responsiveness, but reverse-conducting IGBTs (RC-IGBTs) with internal freewheeling diodes (FWDs) are also under development.[10]

The Approach to New Product Development

The term IGBT indicates a unit-cell structure in an area several microns wide on a silicon chip.

IGBT Technology Trend

NPT-IGBT (1978) (Backside diffusion) MOS-Gate Thyristor type by V-groove
↓ V-Groove: Trench ; Alkali wet etching
↓
PT-IGBT ('80s) 2 layered Epitaxy(n+/n-), Planar Gate, DMOS(Double Diffused MOS)
↓ LSI technology ↑
Planar Gate IGBT(Large SOA type)→ 1um design rule → Submicron design rule
↓ ↓ ↓
Trench Gate IGBT(1um design rule) → **high reliability for Automotive application**
↓
PT-CSTBT(Carrier Stored Trench IGBT)
↓ --- Thin wafer technology ('90s) ---
↓
Thin FZ NPT-IGBT (late '90s) → **RB-IGBT**(Reverse Blocking IGBT)
↓
LPT-IGBT (LPT-CSTBT)→ **RC-IGBT**(Reverse Conducting IGBT)
↓
↓ (1200V class) → HF-IGBT
↓ (600V class) Ultra-thin wafer
↓
↓ --- Future technology (I) (2008) ---
RB-IGBT + RC-IGBT → AC-MOS-Thyristor → AC-IGBT
↓
↓ --- Future technology (II) (2010) ---
SiC Devices (ex. MOS-FET , SBD : Schottky Barrier Diode)
↓
↓ --- Future technology (III) (2020) ---
Diamond Device (ex. FED : Field Emission Diode))
↓

Fig. 4 Technology trends in IGBTs

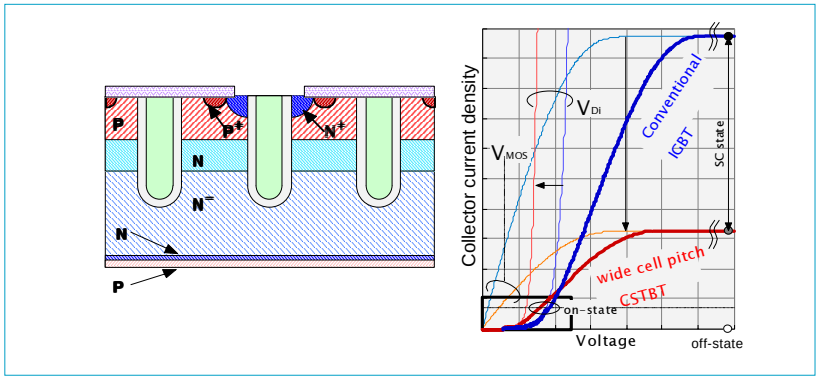


Fig. 5 Operation of IGBTs with the wide cell-pitch structure

The user, on the other hand, thinks of it as a black plastic package several centimeters wide or a dual in-line package (DIP), and the final product characteristics–typically SOA, reliability, durability, etc.–are also viewed as expressions of the device rather than the performance of the chip itself.

Given the above, in the transfer mold-type IPMs in DIPs and in single in-line packages (SIPs), taking advantage of the corporation's proprietary technologies, at least as much effort has been put into the development of the interface technologies between wafer-process and packaging technologies as has been put into the electrical characteristics of the chip itself. This has included several important development themes. For example, lead-free technologies not only require a change in virtually all materials, but when combined with thin-wafer technologies, require radical new technologies in metalization as well. As the flagship of these interfacial technologies, a well-balanced submicron-rule planar gate-type IGBT (Fig. 6) is being developed as a foundation product. Although to some degree the planar gate-type IGBT performance attainable by the given design rule is a little behind the trench-gate one, it serves as an indicator of the overall product performance.

Conclusions

In the low-voltage domain, the performance of trenched-gate MOSFETs has been improved through miniaturization. In the mid-voltage domain, the triangular trade-off among SOA, V_{on}, and E_{off} is helped by leading-edge process technologies while, at the same time, selecting the CSTBT structure (with its increasingly wide cell pitch) or the planar gate structure (with its finest miniaturization) depends on the application. In particular, in the 1,200V class and above, improvements in cost performance are realized by the thin-wafer technologies. In the high-voltage domain, structures and manufacturing methods suitable for parallel connections of the chips are under development, given the potential for high-current applications as well.

Thin-wafer technologies present us with a number of R&D options, such as reverse blocking-type devices and reverse current-type devices.

Although no details can be given here, several structural developments are also under way to improve unexpected oscillations and softness factors in free-wheeling diodes by applying thin-wafer technologies. High-voltage devices, including 6,500V-class devices, will also build on the technologies developed in the mid-voltage domain. ❑

References

[1] A. Narazaki, ISPSD Proc., pages 377 - 380, 2000

[2] A. Narazaki, ISPSD 2004 to be published May 2004

[3] T. Minato, ISPSD Proc., pages 73 - 76, 2000

[4] T. Niita, ISPSD Proc., pages 77 - 80, 2000

[5] H. R. & B. J. Baliga, IEEE Transactions on Electronic Devices, ED-36 (9), pages 1824-1829, 1989

[6] M. Harada, ISPSD Proc., pages 411-416, 1994

[7] H. Takahashi, ISPSD Proc., pages 445-448, 2001

[8] K. Nakamura, ISPSD Proc., pages 299 - 302, 2001

[9] J. Yamashita, ISPSD Proc., pages 421-424, 2001

[10] H. Takahashi, ISPSD 2004 candidate

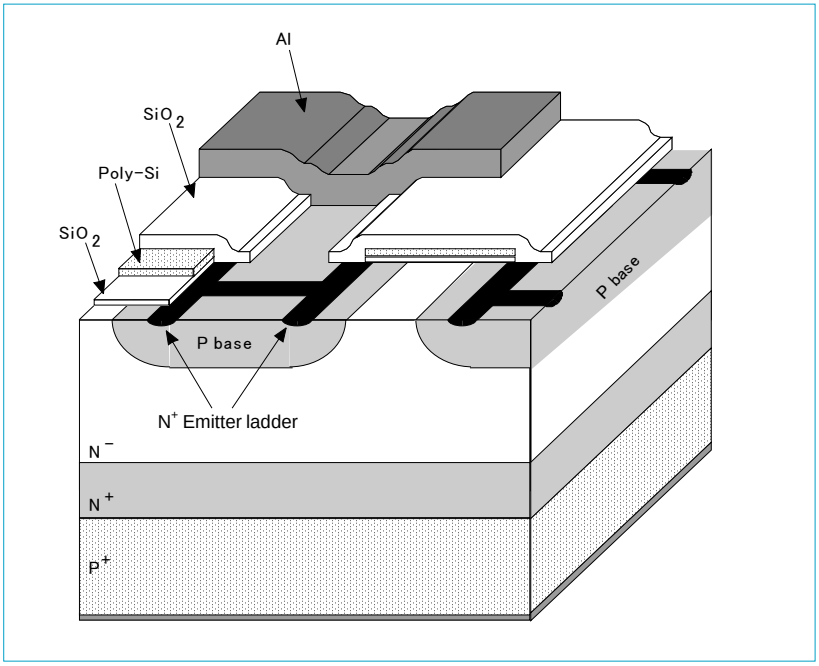


Fig. 6 Submicron-rule planar-gate IGBT

Reverse-Blocking IGBTs for Use in Matrix Converters

Currently, the method most often used to control the frequency of three-phase AC power in equipment for power applications utilizes inverters. The matrix-converter method is the focus of attention as as alternative that will eventually replace this inverter method. Because the switches from which matrix converters are built require reverse-blocking IGBTs which, as their name suggests, can block current in the reverse direction, power devices used for matrix converters have in the past been made from IGBTs in series with diodes.

Mitsubishi Electric Corporation has developed a reverse-blocking IGBT as a power device for use in matrix converters. As shown in Fig. 1, the reverse-blocking IGBT surrounds the IGBT cell region by a deep diffusion-isolation P layer that extends all the way to the back surface, so that the interface between the N^- layer and the P-type collector layer on the back surface is not exposed on the dicing surface. As a result, this structure can block a reverse current because the depletion layer extends from the diffusion-isolation P layer and the P layer on the back surface to the N^- layer when a voltage is applied in the reverse direction.

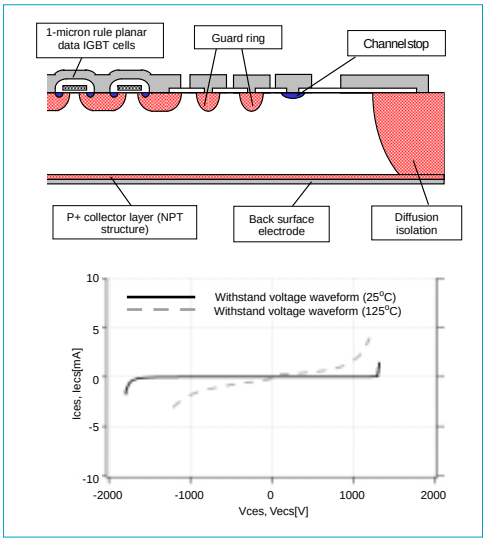


Fig. 1 Cross-sectional view of the reverse blocking IGBT and the breakdown voltage waveforms

The current/voltage waveform when a reverse bias was applied to the reverse-blocking IGBT developed in this project is also shown in the figure. The horizontal axis shows the collector-emitter voltage (V_{CES}) when the gate is shorted to the emitter, and the vertical axis shows the collector cut-off current (I_{CES}). At 25°C, the prototype reverse-blocking IGBT could block voltages of over 1,300V in the forward direction and over 1,500V in the reverse direction. Even at 125°C, the prototype had a blocking capability of 1,200 volts, although there was some increase in the leakage current.

The resulting reverse-blocking IGBT has succeeded in matching the performance of third-generation planar IGBTs in terms of the trade-offs between saturation voltage and switching loss, the key characteristics of an IGBT, while still maintaining the withstand voltage in both forward and reverse directions. These characteristics are obtained through the use of fourth-generation planar MOS structure, along with a shallow P collector on the backside using the corporation's proprietary thin-wafer technology. This reverse-blocking IGBT produces the effect of using a diode, and actual use has confirmed the absence of problems with the equivalent diode properties. The performance achieved by this development gives substantial advantages over that of the conventional structure in which IGBTs are connected in series with diodes. It thus has an important role to play in developing the matrix converters of the future. ❑

IPM L Series with Power Loss Reduction and Noise Reduction

In addition to needs for high performance, compactness, and power-loss reduction in motor-control devices for industrial equipment such as general-purpose inverters and AC servos, recent years have seen regular increases in the requirements for ease-of-use and environmentally-friendly equipment.

Mitsubishi Electric Corporation had already released the S-DASH Series IPM product in response to the demand for these types of power module, and in this development project the corporation has produced its latest IPM product, the fifth-generation L Series IPM. This achieves both power-loss reduction by adopting CSTBT[1] chips in the IPMs and smaller and lighter equipment through the use of a new form of package.

[1] *Carrier-stored trench-gate bipolar transistor: a transistor with an additional carrier-stored layer in the trench gate to improve the trade-off performance between E_{off} and $V_{CE(sat)}$.*

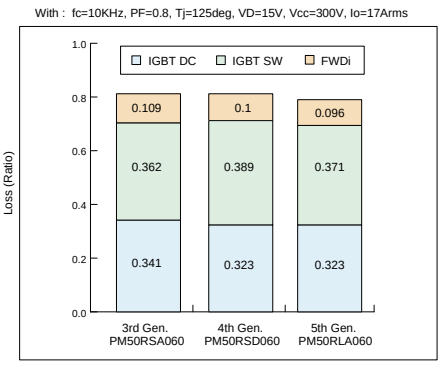


Fig. 1 Comparison of losses in successive generations of Mitsubishi IPMs

Applications

This series is optimized for applications such as miniaturizing inverters in power-source equipment such as UPS units, and for motor-control equipment such as inverter servos for 220V and 440V AC equipment.

It is also applcable to solar-power and wind-power equipment.

Features

1. Low saturation voltage through the application of the fifth-generation new trench chip (CSTBG)
2. The adoption of the new control integrated circuit enables:
   A reduction in the electromagnetic interference (EMI), and
   A major reduction in the current consumption in controlled power supplies.
3. New compact package
4. Increased rated current in the brake parts ❑

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: MITSUBISHI DENKI BLDG., MARUNOUCHI, TOKYO 100-8310, FAX 03-3218-3455