ISSN 1345-3041

VOL. 97/MAR. 2002

MITSUBISHI ELECTRIC ADVANCE

Power Electronics Edition

MITSUBISHI ELECTRIC
Changes for the Better

A Quarterly Survey of New Products, Systems, and Technology
●Vol. 97/March 2002 Mitsubishi Electric **ADVANCE**

Power Electronics Edition

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Cover Story
Our cover shows samples of Mitsubishi Electric power devices that make significant contributions to environmental protection. Main current devices are IGBT modules, which are achieving ever lower switching losses and higher switching speeds. Similar rapid growth is occurring among IPMs, both industrial-use ASIPMs and DIP-IPMs for home appliances. Power capacities of GCTs are also increasing.

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Mitsubishi Electric Advance is published on line quarterly (in March, June, September, and December) by Mitsubishi Electric Corporation.

Overview

The Outlook for Power Devices in the 21st Century

*by Katsuhiro Tsukamoto**

As we face the needs of the 21st century, power electronics and its key components-power devices-are becoming increasingly important in the revolutionary technological developments needed to move to a society based on ecological recycling. This society will make the best use of energy and other Earth resources and make full use of information technology. Progress in power devices has largely centered around insulated gate bipolar transistors (IGBTs) and their main use in controling inverters. The powers that can be controlled by these devices cover a very wide range, from those of a few Watts for switching to Gigawatt-class DC power transmission.

The constant effort to reduce switching losses, improve switching speeds and increase short-circuit ruggedness has resulted in IGBTs of which a fifth generation is now in sight. The intelligent power module (IPM) is largely responsible for the extreme convenience and compact size of power devices by modularizing the circuits needed to operate and protect IGBTs and diagnose their operation. As IPMs with designs optimized to meet market needs in home and industrial appliances, automobiles, locomotives, etc., are developed, the market promises to expand still further.

In the future, there is good reason to believe that silicon will be replaced as the semiconductor material of choice by silicon carbide, and accordingly a great deal of activity is being concentrated in the rapid development of power devices based on MOSFETs, etc., and their practical applications. ❑

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1200V LPT Trench IGBTs

*by Katsumi Nakamura and Shigeru Kusunoki**

Trench insulated gate bipolar transistors (IGBTs) that provide low on-state voltage and low switching losses are already in practical use primarily as 600V- and 1200V-class devices. A newly developed light punch-through (LPT) trench IGBT adopts a novel device structure for further improvements in cost performance and short-circuit ruggedness and a reduction in gate capacity while maintaining the outstanding features of conventional trench IGBTs. This article describes the features and performance characteristics of this new device.

Device Structure

The schematic cross-sections in Fig. 1 compare (a) the usual punch-through (PT) structure, (b) conventional non-punch-through (NPT) structure and (c) the novel LPT structure. Compared with the usual PT IGBT, the NPT type has a markedly different collector structure and generally has the following features:

1. The total substrate thickness (t_{sub}) is thin.
2. The collector is formed of only a shallow and low concentration P layer without any N^+ buffer layer.
3. Since no N^+ buffer layer is formed, the N^- layer is thick.
4. Local lifetime control is not performed for the N^- layer.

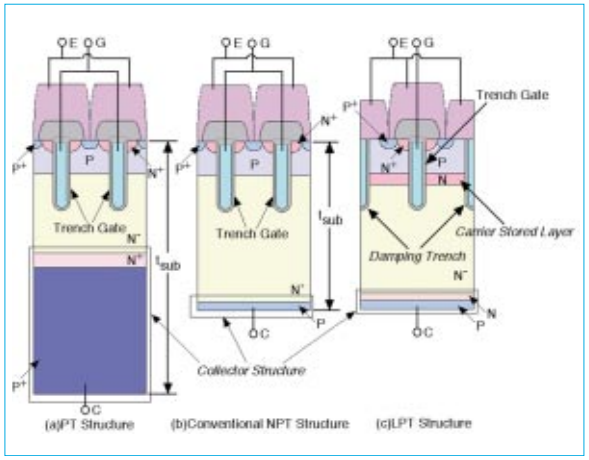

Fig. 1 Schematic cross section of various trench IGBTs.

Accordingly, one problem with the conventional NPT structure has been large losses. These include an increase in leakage current at high temperature (398K), an increase in on-state voltage and large switching loss due to greater tail current at turn-off.

The concept of the LPT trench IGBT is shown in Fig. 2 based on a comparison with a conventional NPT trench structure. This novel 1200V LPT trench IGBT effects the following device structural improvements to resolve the above problems with the conventional NPT structure.

1. A low-concentration N layer is formed on the collector side to suppress leakage current at high temperature and tail current at turn-off.
2. An N layer that serves as a carrier stored (CS) layer[1] is formed directly below the P base for the purpose of reducing the on-state voltage by using the carrier storage effect.
3. A wide cell pitch structure[2] with a large gate pitch has been adopted to improve short-circuit ruggedness and to reduce the gate capacity.

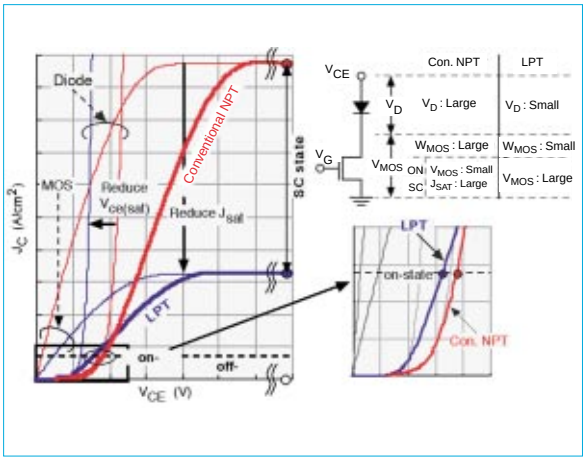

Fig. 2 Concept of wide cell pitch CSTBTs.

As shown in Fig. 2, the wide cell pitch structure reduces the effective MOS gate width (W_{MOS}), thereby suppressing the saturation current (J_{SAT}) and reducing the gate capacity. In addition, the provision of a damping trench suppresses oscillation under short-circuit

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conditions. As a result, high short-circuit ruggedness and a small gate capacity are attained. The adoption of this CS structure lowers the N- layer resistance caused by carrier storage effect and reduces the on-state voltage.

Electrical Characteristics

OUTPUT CHARACTERISTIC AND BREAKDOWN VOLTAGE. The measured I-V characteristics at 298K and 398K for trench IGBTs incorporating the device structures illustrated in Fig. 1 are shown in Fig. 3. Compared with the PT trench IGBT, the I-V characteristic curves of the conventional NPT trench IGBT at 298K and 398K cross at a lower current density, which is effective in preventing device destruction due to thermal runaway. In addition, the LPT trench IGBT achieves a lower on-state voltage than the conventional NPT trench IGBT on account of its increased carrier density due to the formation of the CS layer.

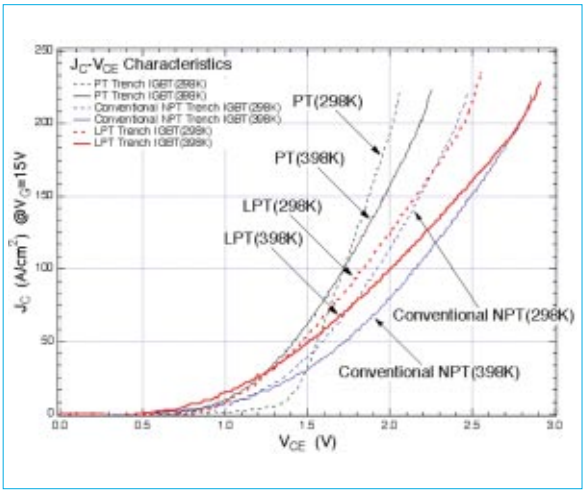

Fig. 3 Measured I-V characteristics of various trench IGBTs.

The junction leakage characteristics measured at 398K for the three different device structures are shown in Fig. 4. It is seen that the leakage current ($J_{C,Leakage}$) of the conventional NPT trench IGBT is twice as great as that of the PT trench IGBT. However, because of the shallow- and low-concentration N layer formed on the collector, the LPT trench IGBT achieves a leakage characteristic approaching that of the PT structure device, enabling it to avoid thermal runaway under high-temperature/high-voltage conditions.

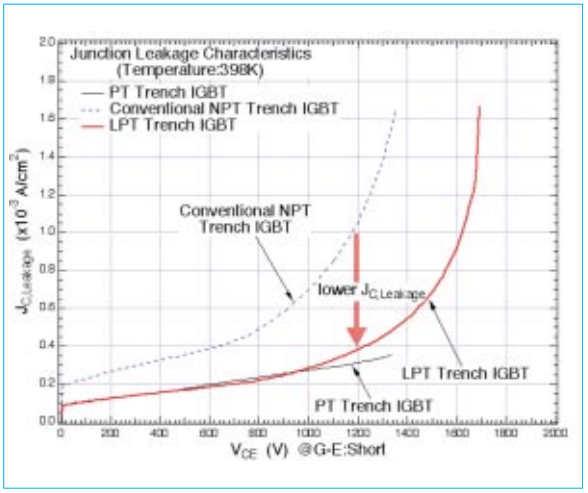

Fig. 4 Measured junction leakage characteristics of various trench IGBTs.

SWITCHING CHARACTERISTIC. Fig. 5 shows the turn-off switching waveforms measured in half-bridge circuits of the three device structures in Fig. 1 under an induction load condition (@V_{CC}=600V, 398K). Compared with the PT trench IGBT, the conventional NPT trench IGBT

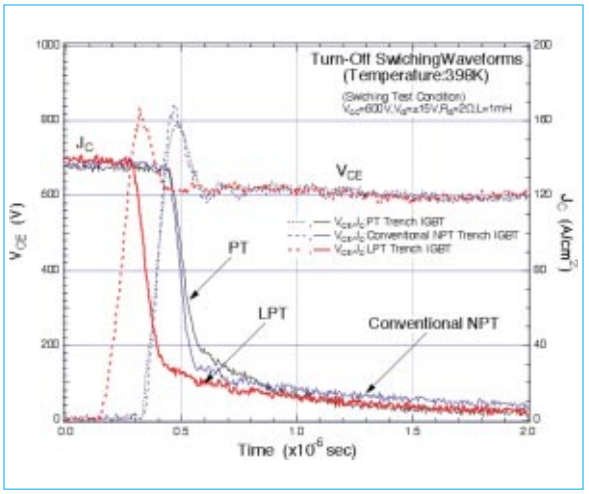

Fig. 5 Turn-off switching waveforms of various trench IGBTs under inductive load condition (@V_{CC}=600V, V_{GE}±15V, R_G=2Ω, 398K).

displays a larger tail current at turn-off. In contrast, owing to its modified collector structure, the LPT trench IGBT attains a low turn-off loss characteristic by suppressing the tail current at turn-off that occurs in the conventional NPT trench IGBT. The LPT trench IGBT also shortens the switching delay time as a result of its reduced gate capacity achieved with the wide cell pitch structure.

SHORT-CIRCUIT RUGGEDNESS. Fig. 6 shows the short-circuit waveforms measured at V_G = 19V for the 1200V LPT trench IGBT with a 15V gate

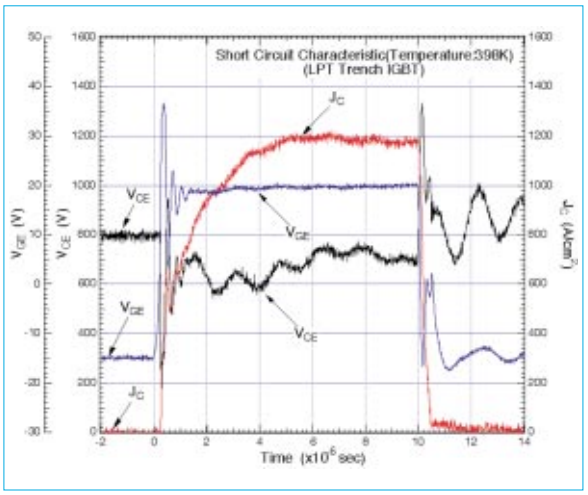

Fig. 6 Short circuit waveforms of 1200V LPT trench IGBT (@V_{CC}=800V, R_G=2Ω, 398K).

driver. The PT trench IGBT and conventional NPT trench IGBT require an overcurrent protection circuit for clamping a short-circuit current to prevent destruction of the device. However, the newly developed LPT trench IGBT features a wide cell pitch structure that reduces the MOS saturation current, enabling the chip itself to achieve better short-circuit ruggedness than conventional trench IGBTs. The measured short-circuit destruction energy (E_{SC}) is E_{SC} = 8.15J/cm^2.

TRADE-OFF CHARACTERISTICS. The trade-off characteristics between the turn-off loss (E_{OFF})and on-state voltage $V_{CE(sat)}$ for the various trench IGBTs in Fig. 1 are shown in Fig. 7. The new LPT trench IGBT achieves a loss characteristic equal to that of the conventional NPT trench IGBT while at the same time maintaining high destruction ruggedness. As seen in the figure, the trade-off characteristic of the LPT trench IGBT has also been improved, thanks to its optimized substrate thickness and emitter resistance. As a result, it provides a device characteristic approaching that of the PT trench IGBT.

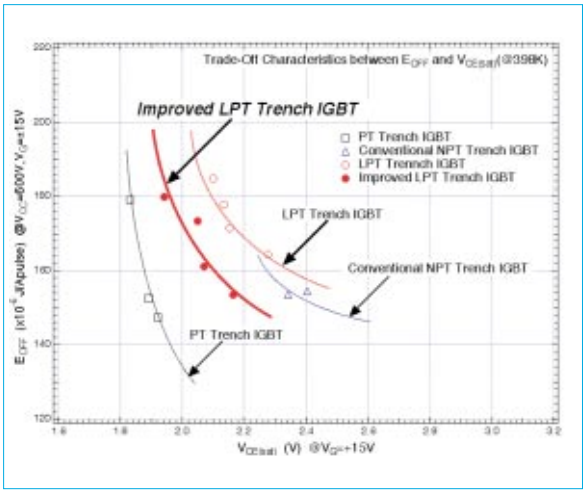

Fig. 7 Trade-off characteristics between on-state voltage ($V_{CE(sat)}$) and turn-off loss (E_{OFF}) for various trench IGBTs.

Owing to its novel device structure, the newly developed 1200V LPT trench IGBT achieves a loss characteristic equal to that of conventional trench IGBTs, high destruction ruggedness on a par with planar gate IGBTs, and reduced gate capacity. As a result, this new device features high overall performance, enabling the gate drive circuit to be downsized and simplified without sacrificing the low loss characteristic of trench IGBTs. The concept of this new device is expected to become the mainstream approach to the development of trench IGBTs developing high voltage power device over voltages of 1200V. ❑

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Intelligent Power ICs: BiC-DMOS

*by Tomohide Terashima and Fumitoshi Yamamoto**

A 0.5µm BiC-DMOS device has been developed that integrates 5~90V bipolar and MOS transistors and 30~90V power MOS transistors with optimized on-resistance. This device process enables the development of ICs for a wide variety of applications, typified by motor control use in automobiles and flat panel display drive circuits.

BiC-DMOS refers to a process technology for integrating CMOS, bipolar transistors and DMOS (NMOS) transistors characterized by high breakdown voltage and large current capacity. Various companies have been working on the development of this process for some two decades now, as the technology offers analog/digital signal processing and power management on a single chip. Process development efforts have been accelerating worldwide over the last few years under the combined effect of two factors in particular. One is the use of fine-pattern technology to attain lower resistance and higher performance for power devices at low cost. The other is greater demand for smaller devices with lower power consumption for such typical applications as mobile communications products. Mitsubishi Electric Corporation has developed a 90V, 0.5µm BiC-DMOS process that is the optimal technology for meeting this demand.

The main devices integrated on a chip with this process are shown schematically in Fig. 1. The use of an optimized structure for the buried diffusion layer on the epitaxial substrate, reduced surface field (RESURF) technology, finer double diffused MOS (DMOS) cells, optimized offset diffusion and 5V/12V gate drive circuits fabricated from 14nm/35nm thick-gate oxide films has made it possible to integrate so many devices and a low on-resistance power NMOS over a wide range of voltages.

Power NMOS

The specific on-resistance of a power NMOS device must be optimized over a broad range of

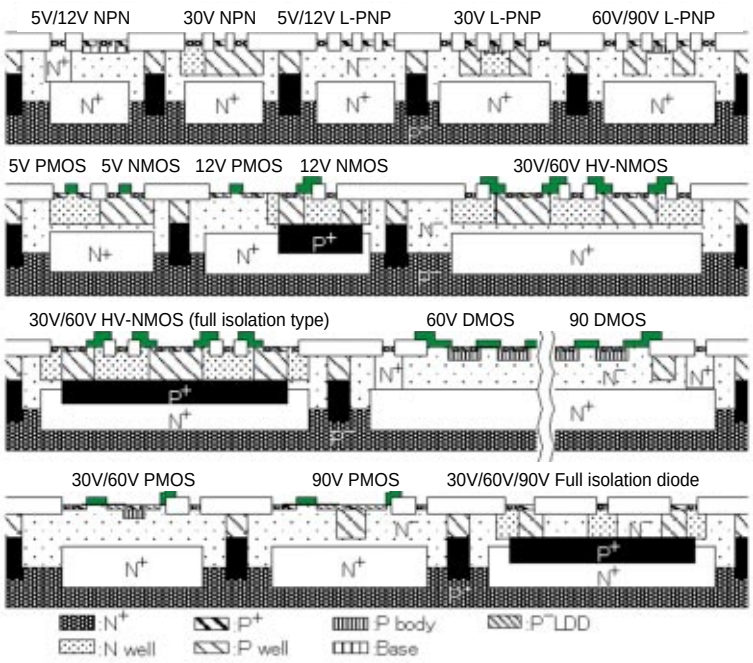

Fig. 1 Schematic views of main devices on BiC-DMOS

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breakdown voltages in order to meet the requirements for lower device costs and applicability to a wide range of applications. To accomplish this, an HV-NMOS was adopted on the low breakdown voltage side and a DMOS on the high side. This facilitated the development of a device with an overall outstanding specific on-resistance characteristic across a wide range of voltages.

DMOS

As the 90V DMOS in Fig. 1 illustrates, a P-well floating ring was added to the field plate above the localized oxidation of silicon (LOCOS) region. This works to reduce the field concentration in the LOCOS region while restricting the device breakdown voltage in the internal DMOS cell region, making it possible to achieve a 90V device. Improvement of the specific on-resistance requires a narrower pitch and a shallower DMOS cell diffusion depth while maintaining the proper P-type body concentration upon which Vth depends. Therefore, a method was adopted for forming the P-type body region by tilt-rotated implantation plus high-energy vertical implantation. As shown in Fig. 2, this resulted in an exceptionally shallow P-type body diffusion depth of less than 1µm and high-density DMOS cell packing (8.2µm pitch). At a breakdown voltage of 95V, specific on-resistance of 130mΩmm^2 was measured in the DMOS cell region. That is an extremely good on-resistance value for a discrete power device by itself.

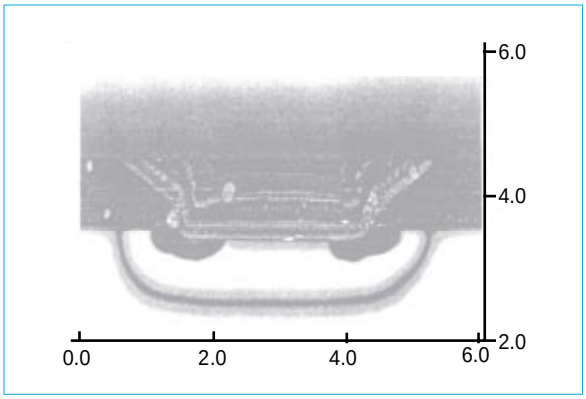

Fig. 2 SCM micrograph of DMOS cell (unit: µm)

DMOS (full isolation type)

With BiC-DMOS devices, inductive load drive is necessary as a power management measure. Consequently, it is necessary to prevent power loss due to parasitic bipolar operation caused by the back-electromotive force of L. A full isolation type DMOS was developed as a device that is capable of minimizing such parasitic operation. A cross-sectional view of the device structure and the electron flow line when back- electromotive force is applied are shown in Fig. 3.

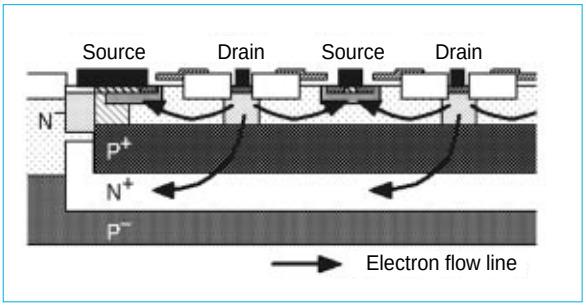

Fig. 3 Cross sectional view of DMOS(full isolation type)

The structure is designed so that the drain is totally surrounded by the P well and P$^+$ buried diffusion layer that become the source potential and by the N well and N$^+$ buried diffusion layer formed on the outside. With this device structure, if the drain potential is less than the source potential, the carriers injected from the drain are electrons and holes are injected from the source only in the direction of the drain electrode. In terms of the operating principle, therefore, the phenomenon of hole current leaking to the P$^-$ substrate does not occur. Measured results show that the leakage current is suppressed to approximately 1/10^7 of the main current. On the other hand, with respect to the breakdown voltage, the RESURF effect of the depletion layer that extends above the P$^+$ burier layer makes it possible to keep the drain-source distance shorter than that of conventional DMOS devices. As a result, the specific on-resistance of the 80V device is superior to that of ordinary DMOS devices.

HV-NMOS

Another method of fabricating a high breakdown voltage NMOS device is the HV-MOS process with the offset drain formed by the N- epitaxial layer and the N well. One advantage stemming from the gentle impurity profile of the pn junction between the P well and the N well is that a high breakdown voltage device can be obtained while maintaining a thin N$^-$ epitaxial layer. Another advantage is that the gate length can be changed to match the circuit by varying the positional relationship between the gate and the P well. Moreover, with the full isolation type HV-NMOS to which a RESURF effect is imparted by adding a P$^+$ buried layer to the lower region of the device, N well depletion is further promoted to yield a device with an even higher breakdown

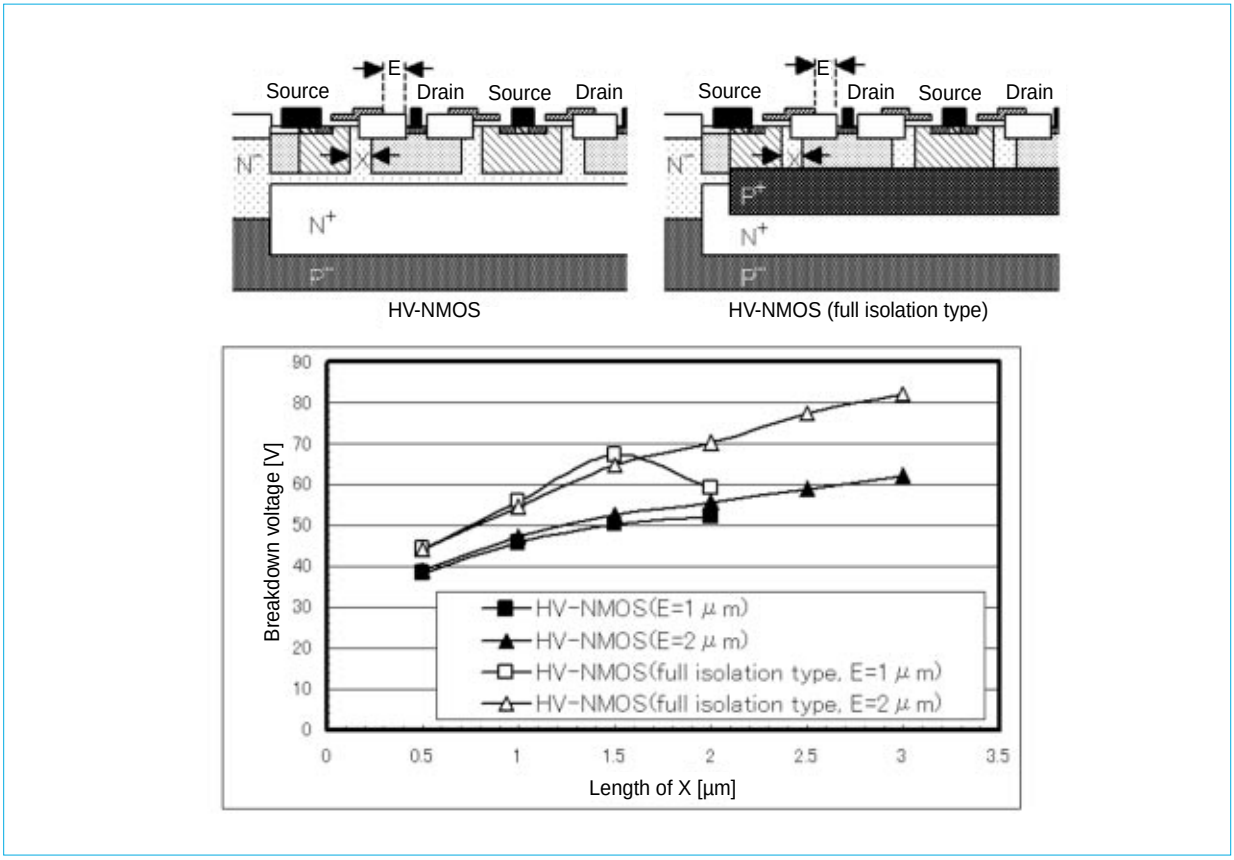

Fig. 4 Relation between the length X and the breakdown voltage

voltage. As shown in Fig. 4, the breakdown voltage increases monotonically in both types of device as X becomes longer. In addition, the RESURF effect increases with higher breakdown voltages. Similar to DMOS devices, a breakdown voltage improvement of approximately 20V is obtained.

Trade-Off with Specific On-Resistance

As indicated in the foregoing discussion, DMOS and HV-NMOS are both available in a standard type and a full isolation type, making a total of four types of device. In real-world applications, the device having the best specific on-resistance characteristic relative to the breakdown voltage of the application is naturally applied. The trade-off between the specific on-resistance and breakdown voltage is shown in Fig. 5 for all of the devices. The curve of each device plots the change in this relationship accompanying a change in the breakdown voltage hold structure (e.g., source-drain distance, etc.). There is evidently an optimum breakdown voltage region for each device. As a result, as the power NMOS of the BiC-DMOS, the 90V, 80V, 60V and 40V devices adopt a DMOS, a full isolation type DMOS, a full isolation type HV-NMOS and an HV-NMOS, respectively.

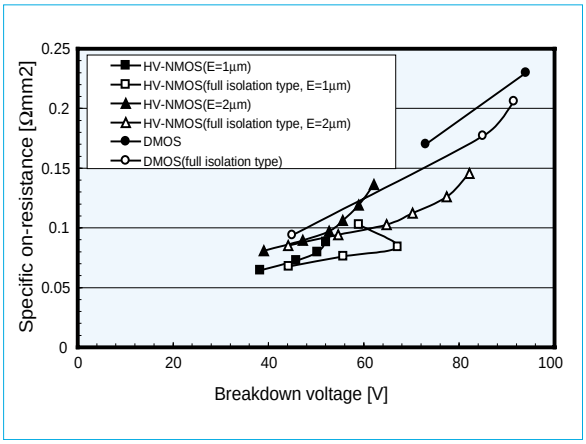

Fig. 5 Trade-off relation between specific on-resistance and breakdown voltage

The corporation's new lineup of BiC-DMOS devices now makes it possible to provide a series with the best on-resistance characteristics to match the desired breakdown voltages of a wide range of specific applications. ❑

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T. Terashima, F. Yamamoto and K. Hatasako, "Multi-voltage device integration technique for 0.5µm BiCMOS & DMOS process", Proc. ISPSD, pp. 331-334, 2000.

Sixth Generation Low-Voltage MOSFETs with Low On-Resistance

*by Atsushi Narazaki and Katsumi Uryuu**

Mitsubishi Electric Corporation has developed the sixth generation of low-voltage trench gate MOSFETs designed for battery-control use in mobile communications devices. Featuring a trench gate structure with a 0.35µm design rule and a 2.5V gate drive, these latest generation MOSFETs provide low on-resistance and high destruction immunity. Compared with fifth-generation MOSFETs using a 0.6µm design rule, the cell density has been increased and the on-resistance has been reduced by approximately 25%.

Power MOSFETs with low breakdown voltage have traditionally been used in office-automation equipment and in switching applications such as DC/DC converters and switching power supplies. In addition, as a result of the recent diffusion of mobile communications devices, they have also found extensive application as power-management circuits and as protection circuits for lithium-ion batteries. These applications require a low-voltage drive circuit capable of being driven directly from the battery and reduced on-resistance for minimizing loss while current flows.

A general approach to reducing on-resistance is to improve the current capacity by increasing the cell density through a reduction in the unit cell size. However, this approach requires the use of complex fine-pattern technology, which can give rise to the problem of lower yields in the manufacturing process. Another inherent problem of MOSFET device structure is that devices are apt to be destroyed by the accumulated energy of the circuit's own floating inductance during switching at high frequencies. The newly developed sixth generation power MOSFETs with low breakdown voltage overcome these problems by incorporating techniques described below and utilize unique fine-pattern technology to achieve high destruction immunity with low on-resistance. The specific on-resistance ($R_{on,sp}$) of the new devices is 18mΩµm^2 at V_{GS} = 4V, which is approximately 25% lower than that of the previous generation.

Reduction of On-Resistance

For 20V-class power MOSFET chips, channel resistance accounts for approximately 68% of the total resistance, excluding substrate resistance. In the case of low breakdown voltage power MOSFETs, reducing channel resistance is the most effective way of lowering chip resistance.

Fig. 1 shows the specific on-resistance ($R_{on,sp}$) of two generations of power MOSFETs as a function of their normalized unit cell size. These results were obtained by using a certain test pattern. Table 1 compares the cell densities of the sixth and fifth generations of power MOSFETs.

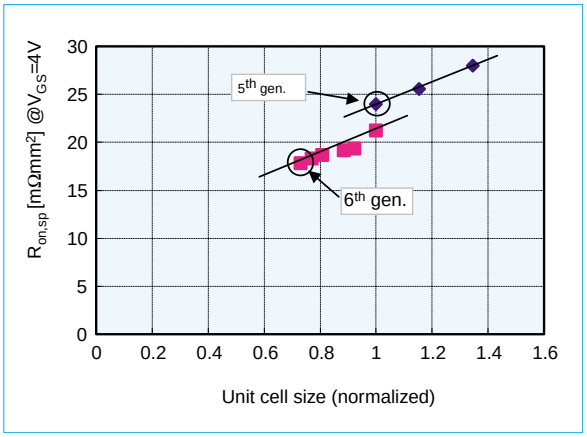

Fig. 1 The relationships between the normalized cell size and $R_{on,sp}$

Compared with the fifth-generation devices, the new sixth-generation MOSFETs have a larger specific channel width (i.e., total channel area) for the same cell size. This was accomplished by narrowing the trench width, making it possible to reduce channel resistance and thereby also to lower the on-resistance of the chip. Moreover, reducing the unit cell size increased the cell density for an improvement in current capacity and a reduction of on-resistance.

The design of the sixth-generation MOSFETs features a trench width of 0.35µm, obtained with the same level of fine-process technology as that of the fifth-generation device design. This was accomplished by using a process technology originally developed by the corporation to form the trench pattern of the unit cell. As a result,

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compared with the fifth-generation devices, the cell size has been shrunk by 27% and the cell density has been increased by 87% (Table 1).

Table 1 The Comparison of Cell Densities (relative value)

	Trench width (μm)	Unit cell size	Total channel width	Cell density
5th gen.	0.6	1	1	1
6th gen.	0.35	0.73	1.41	1.87

Improvement of Destruction Immunity

Reducing the cell size lowered the on-resistance, but it was necessary to resolve the decline in performance and yield that occurred owing to the insufficient pattern margin resulting from the finer pattern.

Fig. 2 shows a cross-sectional view of the cell structure of a power MOSFET with a trench gate structure. Reducing the cell size narrowed the

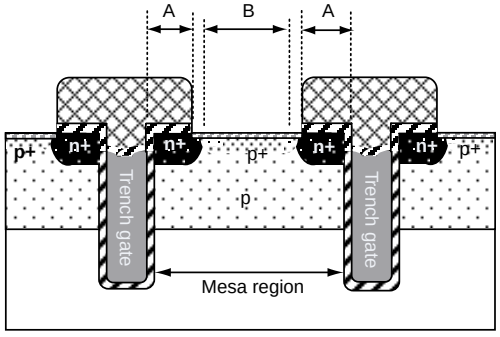


Fig. 2 The cross sectional view of the unit cell

silicon mesa region separated by the mesh-pattern trenches. However, taking into account the following problems, it is desirable to design a wide silicon mesa region:

1. Gate defects caused by the insufficient overlap margin between the trench gates and source contact holes (Fig. 2 (a))
2. Decline in avalanche destruction immunity during unclamped inductive switching due to the smaller p+ contact size (Fig. 2 (b))

The narrower trench width adopted for the newly developed sixth-generation MOSFETs made it possible to secure the same overlap margin between the trench gates and source contact holes and also the same p+ contact size as the fifth-generation devices. That enabled the on-resistance to be reduced without degrading either the gate yield or avalanche destruction immunity. Moreover, as shown in Fig. 3, destruction immunity was also improved at the same time due to the avalanche current dispersion effect of the higher cell density.

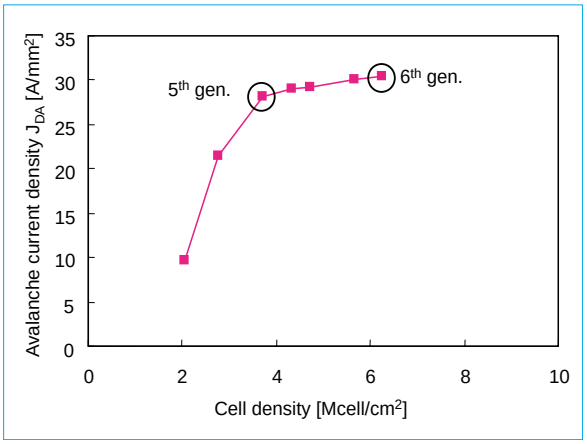


Fig. 3 Dependence of the avalanche current density on the cell density with the same p+ contact size.

Device Characteristics

The graph in Fig. 4 shows the dependence of the specific on-resistance ($R_{on,sp}$) on the gate volt-

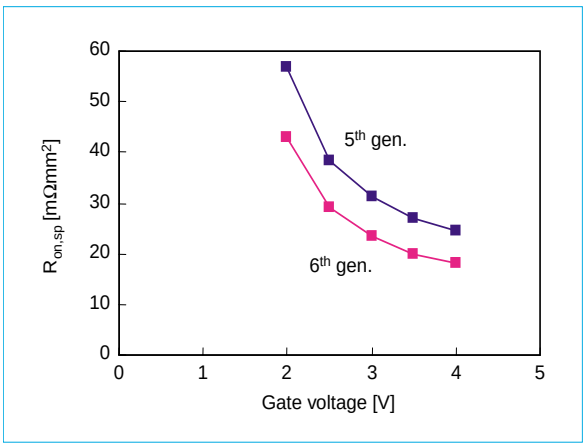


Fig. 4 Dependence of $R_{on,sp}$ on the gate voltage.

Table 2 Characteristics of 5th and 6th Generation MOSFETs

	V_{dss} (@I_d=0.1mA) (V)	V_{th} (@I_d=1mA) (V)	$R_{on,sp}$ (@V_{GS}=4V) (mΩ • mm²)	$R_{on,sp}$ (@V_{GS}=2.5V) (mΩ • mm²)	J_{DA} (T_C=150°C) (A/mm²)
5th gen.	30	0.8	25	38	28
6th gen.	28	0.75	18	29	32

age. The major characteristics of the fifth- and sixth-generation MOSFETs are compared in Table 2. The newly developed sixth-generation MOSFETs display specific $R_{on,sp}$ of 18 mΩμm² at V_{GS} = 4V. Compared with the fifth-generation devices, on-resistance has been reduced by approximately 25%. In addition, the new devices also provide avalanche destruction immunity of JDA = 30A/mm² at Tc = 150°C during unclamped inductive switching. This performance stems from their amply large p^+ contact size and higher cell density achieved with the fine-pattern process providing a 0.35μm design rule.

The corporation's newly developed sixth-generation power MOSFETs can contribute to extending the battery life of mobile devices and to energy-saving systems by making the most of their features such as low on-resistance and high destruction immunity. We plan to create a series of devices with varying drive voltages and breakdown voltages in order to meet a broad range of market needs. ❑

Transfer Mold-Type IPMs for Driving Small-Power Motors

*by Mitsutaka Iwasaki and Toru Iwagami**

Mitsubishi Electric Corporation has been commercializing transfer mold-type dual-inline package intelligent power modules (DIP-IPMs) for the inverter-driven home appliances market. We are now developing a DIP-IPM series featuring improved functionality and reliability to meet more rigorous market requirements. This article describes the design technology and major features of this series.

DIP-IPM Series and Applications

Products in the DIP-IPM series come in two types of packages-large or small-to match the current rating of the intended application. Large-package modules are used for air-conditioner compressors driven by power chips of the 12~25A/600V class, and small-package modules are used for driving washing machine motors and refrigerator compressors that employ power chips of the 3A/500V~10A/600V class. The external appearances of the large- and small-package DIP-IPMs are shown in Figs. 1 and 2, respectively.

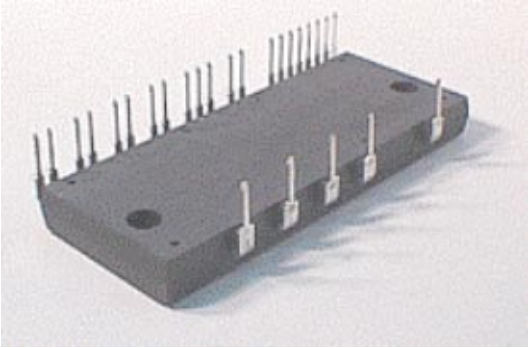


Fig. 1 The larger transfer-mold IPM package. Mold size is 79 x 31 x 8 mm.

Functions of DIP-IPM Series

The major functions and features of the DIP-IPM series are described below.

POWER CIRCUIT. The three-phase inverter consists of IGBTs and associated free-wheeling diodes (FWDs).

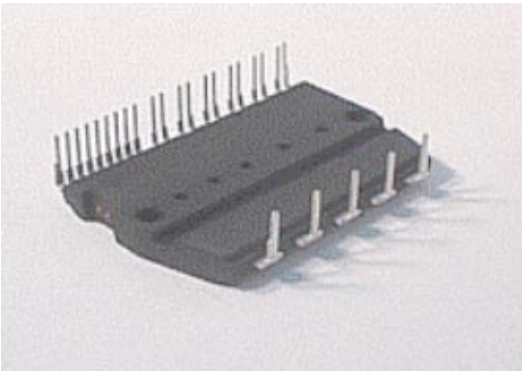


Fig. 2 The smaller transfer-mold IPM package. Mold size is 49 x 30.5 x 5 mm.

CONTROL IC. This contains the drive circuit for the P-side IGBTs, a high-voltage level-shift circuit and a control supply under-voltage (UV) protection circuit, although without any error output. For the N-side IGBTs, it includes a drive circuit and a short-circuit protection circuit (with Fo). It also contains an N-side control supply UV protection circuit (with Fo). An internal block diagram of a small-package DIP-IPM is shown in Fig. 3.

Key Technologies

POWER-DEVICE CHIP TECHNOLOGY. The DIP-IPM series achieves lower loss levels by adopting fourth-generation planar structure IGBTs. By applying fine pattern technology to the IGBTs and vertically oriented lifetime control technology, collector-emitter saturation voltage has been reduced by approximately 10% and the inverter loss (three-phase sine-wave control) by approximately 8% compared with the performance of third-generation planar structure IGBTs.

ASIC TECHNOLOGY. The DIP-IPMs represent an all-silicon solution, consisting only of IGBTs, FWDs and drive ICs. A frame configuration has been adopted for the circuit wiring to reduce self-inductance and the generation of noise. This

**Mitsutaka Iwasaki and Toru Iwagami are with Power Device Division.*

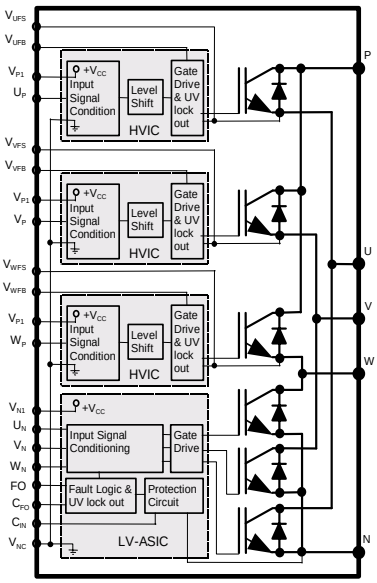


Fig. 3 Internal block diagram of the smaller transfer-mold DIP-IPM

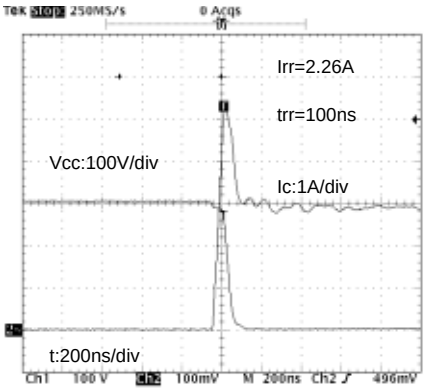
measure to prevent noise in the ICs has made it possible to reduce the number of noise filters used.

PACKAGE TECHNOLOGY. The establishment of transfer mold technology has resulted in more compact power modules. In addition, optimization of the frame structure and the use of a plastic material with excellent heat radiation and conduction properties have achieved a high heat radiation characteristic.

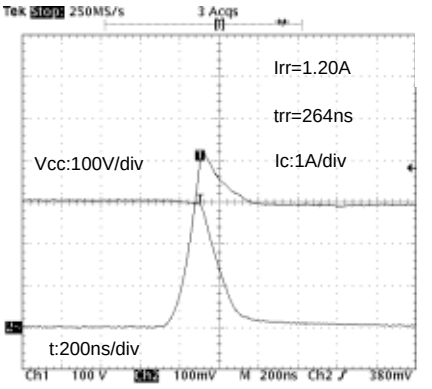
Features of DIP-IPM Series

LOWER NOISE. Lower noise levels are required of home appliances used indoors in order to reduce the effect of any noise generated upon nearby electronic products. For the N series of small-package DIP-IPMs, the collector-emitter saturation voltage of the IGBTs was reduced, making it possible to optimize the turn-on speed, which is one cause of noise, and to improve the recovery characteristic of the FWDs.

As a result, an in-house evaluation has confirmed that the conducted emission level has been reduced by more than 10dB in the 8~10MHz frequency band, for example, compared with that of previous devices. This improvement allows fewer noise-control components to be used, reducing system cost. Fig. 4 compares the turn-on waveforms of a conventional device and a low-noise device.



(a) Previous product (PS20351-G)



(b) Low-noise product (PS20351-N)

Fig. 4 Turn-on waveforms

REDUCTION OF ARM SHORT-THROUGH LOCKING TIME. White goods installed indoors often have their carrier frequency set high on account of noise considerations. In this case, the arm short-through locking time when the motor is being driven can have a variety of undesirable effects, including a decline in motor output, an increase in torque pulsations and unstable operation. By optimizing the switching time and the delay time of the control IC, the arm short-through locking time of the small-package DIP-IPMs has been reduced to 1.5µs.

ENHANCED FUNCTIONALITY. Previously, the approaches taken for over-temperature (OT) protection have included the attachment of a thermistor to the heat-radiation fin of a DIP-IPM to detect the temperature. However, it has become necessary to incorporate an OT protection function within DIP-IPMs. To meet this requirement, DIP-IPMs with a built-in OT protection function have been added to the product lineup.

IPM with New Package Construction

There are strong demands for further reductions in device size, especially in the small-power motor market such as the segment for refrigerator and air-conditioner fan motors. In response to that demand, we are developing a single-inline package IPM (SIP-IPM)with vertical mounting. This SIP-IPM is shown in Fig. 5. Vertical mounting reduces the mounting area of a large-package DIP-IPM by approximately 90% compared with that of previous devices. It also has the advantage of facilitating easier peripheral wiring by separating the high- and low-voltage terminals on the two sides. The major functions and features of the SIP-IPM are described below.

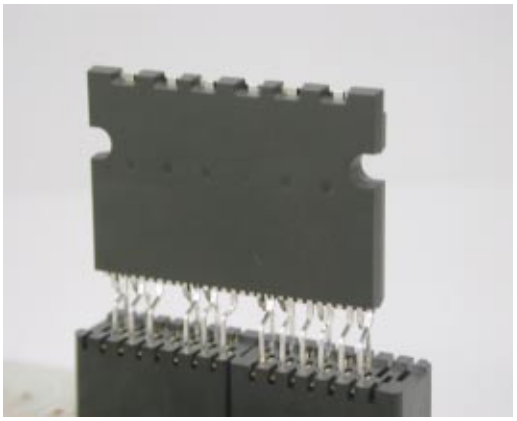


Fig. 5 The SIP-IPM

ENHANCED FUNCTIONALITY. In addition to the features of the small-package DIP-IPMs, this new device incorporates arm short-through interlock protection for improved reliability by preventing arm shorts due to spurious signal inputs, noise or other causes.

LOSS REDUCTION. Next-generation planar IGBTs with a 0.6µm design rule for reduced collector-emitter saturation voltage and low-VF FWDs have been adopted to achieve lower power losses. In addition, the supply current of the ICs has been reduced by approximately 50% compared with existing devices.

HIGHER EFFICIENCY. An arm-short-through locking time of 1µs has been attained.

Inverters are being applied in a wide range of areas in the home appliances market today, extending from 50W-class fan motors to 2.2kW-class or larger motors for the compressors of air-conditioning units. Moreover, it is expected that the requirements for power modules will become increasingly rigorous due to regulations governing energy savings and higher harmonics, recycling legislation and other factors. Against this backdrop, we intend to develop new packages that revolutionize previous concepts as well as low-loss power chips. ❑

Reference

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Advances in Integrated Intelligent Power Modules for Hybrid Electrical Vehicles

*by Masakazu Fukada and Hirotoshi Maekawa**

Mitsubishi Electric intelligent power modules (IPMs) have been adopted in various general purpose and industrial applications all over the world. For hybrid electric vehicle (HEV) applications, the high temperature and other environmental conditions in the engine room subject the IPM to severe stress. HEVs are expected to account for 10% of the world's total vehicle production by the year 2010 and, in addition to improved IPM electrical characteristics, durability and cost-performance are very important factors for the future. This article introduces a next-generation IPM system model with detection, protection and control features and a built-in smoothing capacitor. This embodies advanced integration and miniaturization, forming an intelligent integrated power-drive unit (IPU). New technologies enable the IPU concept to achieve high durability and reliability without using special high-temperature resistant materials.

Improving Power-Module Reliability for HEVs

POWER-MODULE HEAT CYCLE. Unlike pure electric vehicles (EVs) which have no engine, the high engine-room temperatures of HEVs impose severe heat cycle (H/C) conditions on the power module. Therefore, the use of a copper compound base-plate metal material with a low linear expansion coefficient is indispensable to satisfy the H/C requirements. Such materials were successfully adopted in the second generation HEV-IPM (CGA Series), but for the newly developed IPU (third generation HEV-IPM) the severe heat-cycle target specifications (-40 ~125°C for at least 1,000 cycles) were achieved through the use of a copper base plate with superior heat-transfer characteristics. The major improvements achieved are as follows.

CHIP LAYOUT OPTIMIZATION. As illustrated in Fig. 1 (a), the conventional layout subjects the power chip to high temperature rise with the slightest solder-crack at the corners (due to unbalanced heat dissipation), and this promotes further extension of the solder crack. Through the use of electromagnetic thermal-stress simulation, the chip layout was optimized for minimal chip thermal stress on the solder between the ceramic plate and the base plate near the corner as shown in Fig. 1 (b). Thus, the new layout extends the time until the power chip experiences increased thermal stress even if a solder crack occurs near the corner. As a result, deterioration in the junction-to-case thermal resistance was inhibited, meeting the H/C requirements and improving thermal-stress endurance.

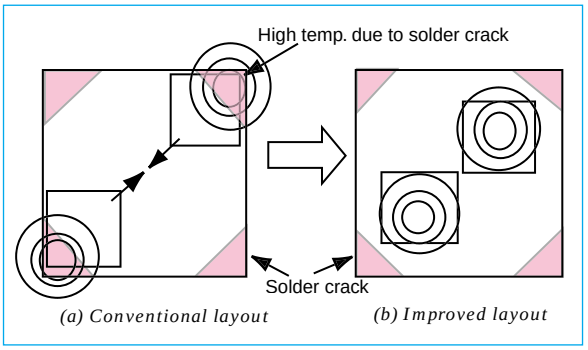

Fig. 1 Chip layout optimization

SOLDER CONTROL. Solder thickness is known to exert a powerful influence on the power module's ability to satisfy H/C requirements. As shown in Fig. 2 (a), increased solder thickness improves the ability to endure cracks but in conventional designs it proved difficult to secure reasonable and uniform solder thickness. This is evident from Fig. 2 (b), which shows solder thickness distribution

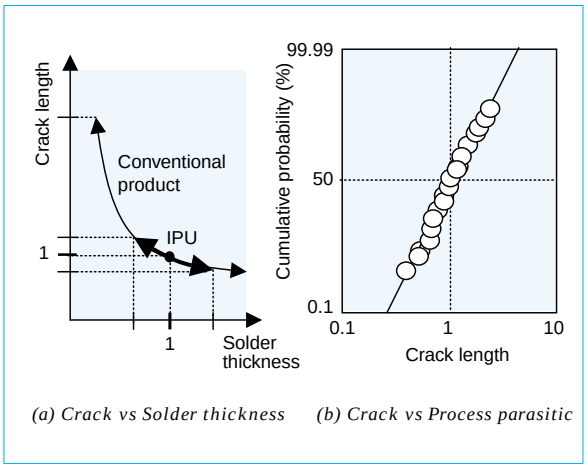

Fig. 2 Effect of solder thickness on the crack length

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(neglecting other process parasitic factors). This means that the highest concentration of thermal stress occurs at the thinnest part of the solder layer, which in turn determines the H/C capability.

In the newly developed IPU, variations in the thickness of ceramic-plate solder were limited (ensuring the minimum necessary thickness) by highly precise soldering, and enforced parasitic control, thus extending the period before solder-crack occurrence and establishing suitable production conditions to satisfy the H/C requirements.

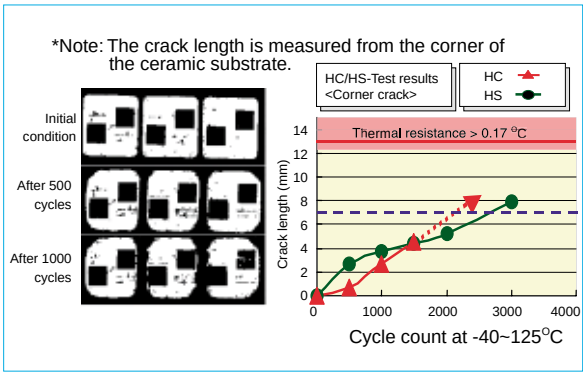


Fig. 3 Heat-cycle and heat-shock test results.

ON-CHIP TEMPERATURE SENSOR. The IPU is fitted with an on-chip temperature sensor that quickly reports the temperature and guarantees fail-safe IPU operation even if a solder crack propagates despite the optimized chip layout, as will be evident from Fig. 4 (a) and Fig. 4 (b). Conventionally, various materials with low linear expansion coefficients were used to satisfy high H/C requirements, but we have established technology enabling the IPU to safely satisfy severe H/C requirements (-40~125°C for at least 1,000 cycles) by utilizing a copper base plate.

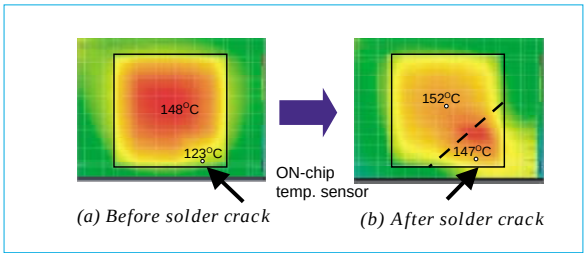


Fig. 4 Chip-temperature distributions.

Thus, since the base-plate thermal conductivity was improved by about 1.5 times when compared with traditional composite materials with low linear expansions, it became possible to increase the current density even using the same chip.

POWER CYCLE. Functional integration is expected to increase in the future, and high-performance water cooling is being considered as a possible replacement for air-cooling in the implementation of compact HEV-IPMs with large current capacity. In conventional industrial and general-purpose IPM designs utilizing air-cooling fins, the ΔT_{jmax} values have been set at around 30°C. On the other hand, for high capacity HEV-IPMs with water-cooled fins, since ΔT_{jmax} values of at least 50°C are expected, wire-bonding improvement becomes important in order to satisfy the power cycle (P/C) requirements. For the newly developed third-generation HEV-IPM (IPU), optimization of the chip-electrode metallization and wire bonding is planned to produce at least a two-fold P/C improvement over the traditional third generation HEV-IPM (with $DT_j = 50°C$). Further, with the help of optimized wire bonding, an improvement in T_{jmax} of about 10°C has been achieved as shown in Fig. 5 (a). The resulting P/C has a favorable increase of an order of magnitude under rated current and actual operating conditions, as shown in Fig. 5 (b).

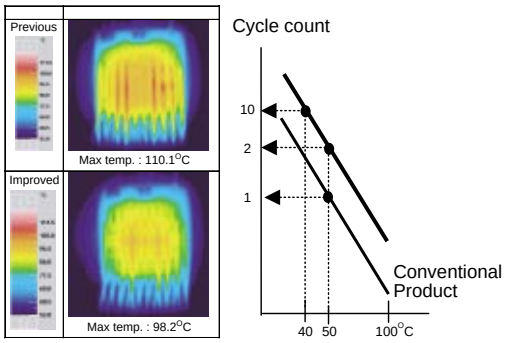


Fig. 5 Chip temp. reduction and power-cycle improvement

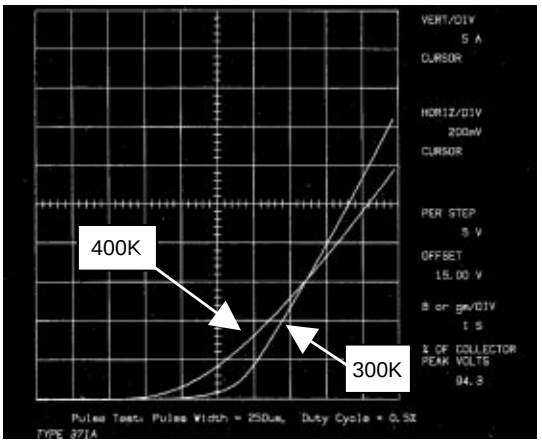
The Power Chip

Sub-micron design rule was adopted for the IGBT chips exclusively developed for this IPU, thus allowing chip miniaturization without lowering the saturation current level. Variations in the gate-threshold level were carefully addressed allowing sufficient margin for safe inverter operation. Further, due to the low power losses of the new chips under actual operating conditions, it was possible to raise the current density to 200A/cm^2.

Anti-noise measures were considered in the IPU switching characteristics leading to an optimized performance level equivalent to that of the fourth-generation power chips. Ultrasoft-recovery free-wheeling diode chips were also developed for the IPU.

Super-Fine Planar Gate IGBTs

Because of the severe conditions under which HEV IPMs operate, caution is necessary when designing the IGBT gate drive power supply with respect to control-board temperature increases. This is particularly true for high capacity IPMs (rated at several hundred amperes) where the high gate capacitance cannot be ignored. Further, to overcome ground-potential variations of each IGBT arm, six isolated drive power supplies were integrated within the IPU; therefore in order to achieve a low IGBT gate capacitance, the super-fine planar IGBT gate structure was adopted. The low ON-voltage characteristics of the developed IGBT chip are shown in Fig. 6 and Table 1.



Y-axis : 50A/cm^2 X-axis : 0.2V

Fig. 6 IGBT ON-voltage characteristics

Table 1 IGBT Saturation Voltage Comparison

IGBT generation	Design rule	VCE(sat) @200A/cm^2	Unit-cell size
3rd Planar	3µm	2.7V	1
4th Planar	1µm	2.0V	0.6
5th Planar	Sub-µm	1.6V	0.5
4th Trench	1µm	1.5V	0.1

Future Developments

Through the improvements achieved in the IPU development, it is possible to meet the requirements of 55kW motor applications (400A-class) utilizing only one chip instead of the conventional two-chip parallel standard module style shown in Fig. 7. With conventional low linear expansion coefficient composite materials it is difficult to achieve high current densities because the lateral heat-transfer performance is poor and high temperatures are concentrated directly under the power chips. This is particularly true when the thermal-grease layer between the base plate and the cooling fin transforms into oil locally beneath the power chips (due to the high temperatures there) and resulting in even worse thermal-transfer characteristics. Development of a water-cooled IPU module that dispenses with thermal grease is planned. Such a module will be capable of supporting 360A rms rated output current with only one chip, as suggested by the simulation results shown in Fig. 8.

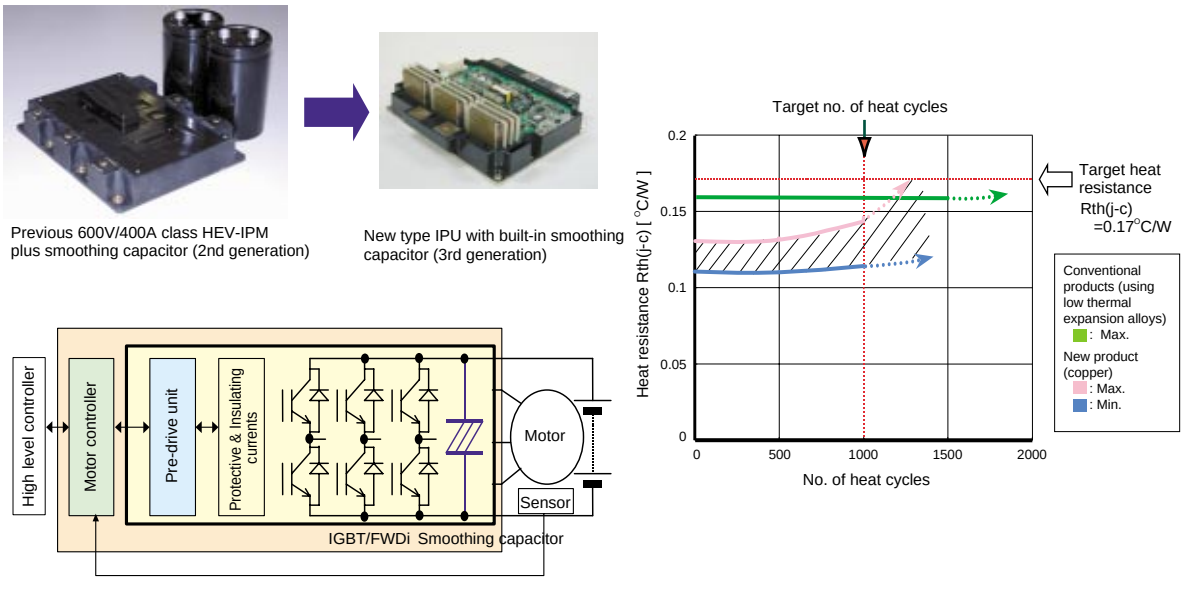


Fig. 7 Conventional HEV-IPM and IPU (prototype) at – 40~125°C on a 15 x 15mm IGBT chip

This IPU development achieved high functional integration in a compact intelligent module for HEV applications. High reliability and high durability were achieved without using special base-plate materials thus greatly improving the cost-performance figures. The IPU represents a technical initiative aiming at lower losses, compactness and effective high productivity. The IPU seems sure to make a positive contribution to the future spread of hybrid-electric and electric vehicles. ❑

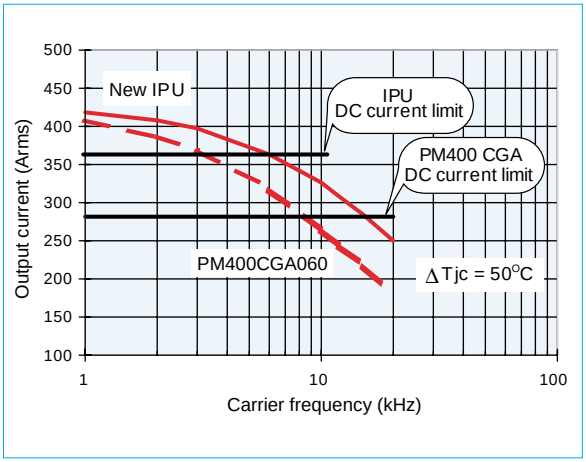


Fig. 8 IPU simulated output current capability

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4.5kV HVIGBT Series Modules

*by Satoru Chikai and Koichi Mochizuki**

Mitsubishi Electric Corporation has used an optimized design for IGBT chips to develop 4.5kV (rated voltage) HVIGBT modules with a saturation voltage between the collector and emitter lower than the 3.3kV of the corporation's previous products. Three new products of this types have now been released, with rated currents of 400A, 600A and 900A.

Development Targets

Semiconductor devices able to withstand increasingly high voltages are needed in order to make power systems smaller and lighter in the field of high-voltage applications. In response, the corporation will release the new products in the same package types as the 2.5kV/3.3kV HVIGBT modules previously released. One goal in the project was to reduce the saturation voltage between the collector and the emitter to a value lower than the 4.0V saturation voltage in the 3.3kV HVIGBT module (at the rated collector current and a junction temperature of T_J=125°C).

Description of the Modules

Fig. 1 is a view of the 4.5kV HVIGBT module. On the left is a 400A/600A single HVIGBT module, measuring 38 × 140 × 130mm (H × W × L), the same as the 2.5kV/3.3kV, 800A product. On the right is the 900A single HVIGBT module, measuring 38 × 140 × 190mm, the same as the 2.5kV/3.3kV, 1200A product.

When designing high-voltage IGBT chips, the n⁻ base layer thickness must be increased to suppress the hot leakage current (to prevent thermal runs); however, because this has a negative effect on the boundary between the switching loss and the collector-emitter saturation voltage, the design used reduced the thickness of the n⁻ base layer as far as possible.

Fig. 2 shows the dependencies of the collector-emitter saturation voltage $V_{CE(sat)}$ and the hot

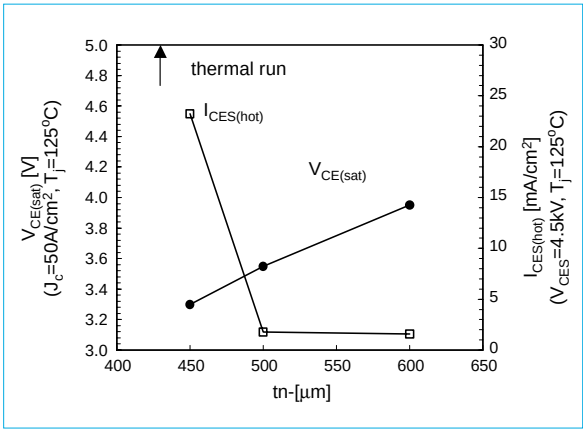

Fig. 2 Dependence of $V_{CE(sat)}$ and $I_{CES(hot)}$ on t_{n-} in the 4.5kV-IGBT chip

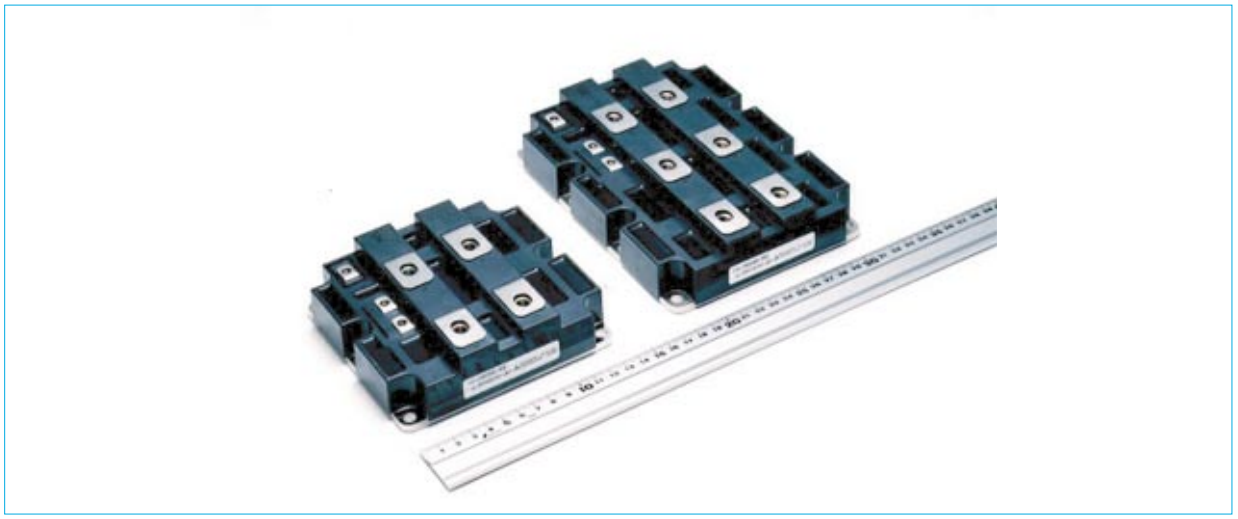

Fig. 1 4.5kV HVIGBT modules

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leakage current $I_{CES(hot)}$ on the n⁻ base layer thickness t_{n-} in the conventional IGBT chip structure.

Although it is evident from Fig. 2 that a design with T_{n-} = 500µm would cause $V_{CE(sat)}$ = 3.6V, fulfilling the original target value of 4.0V, the results of other investigations made it clear that $I_{CES(hot)}$ could be reduced by optimizing the density in the p⁺ collector layer, so the development target was changed to $V_{CE(sat)}$ = 3.3V, and a thickness of t_{n-} = 450µm was selected. Note

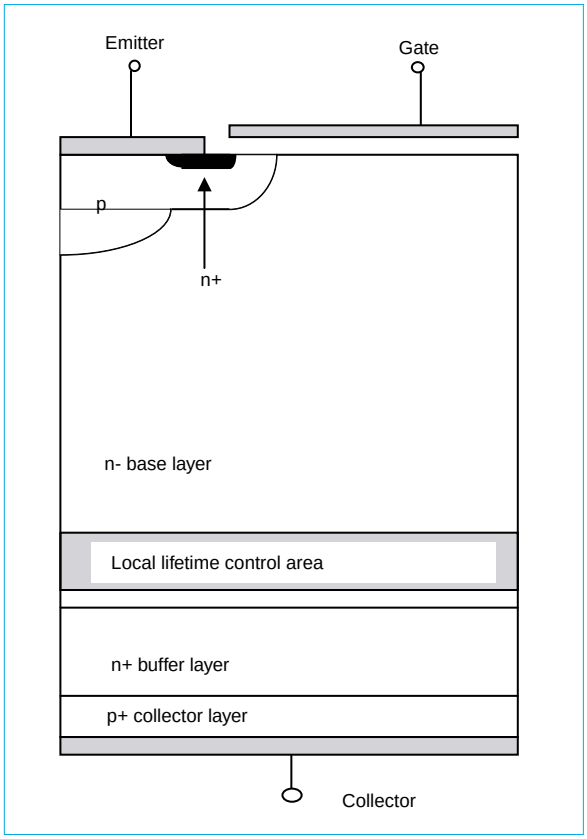

Fig. 3 Cross-section of the high-voltage IGBT chip

that Fig. 3 shows the structure of the high-voltage IGBT chip.

After these investigations, further investigations were performed to optimize the p⁺ collector layer density in order to suppress $I_{CES(hot)}$. Fig. 4 shows the dependence of the collector-emitter saturation voltage $V_{CE(sat)}$ and the hot leakage current $I_{CES(hot)}$ on the density ratio γ of the densities of the p⁺ collector layer and the n⁺ buffer layer ($=C_{S(p+)}/C_{S(n+)}$).

Taking into consideration the balance of $V_{CE(sat)}$ and $I_{CES(hot)}$ in the graph of Fig. 4, a γ of between 10 and 15 was selected. The result was the ability to reduce $I_{CES(hot)}$ while avoiding any increases in $V_{CE(sat)}$.

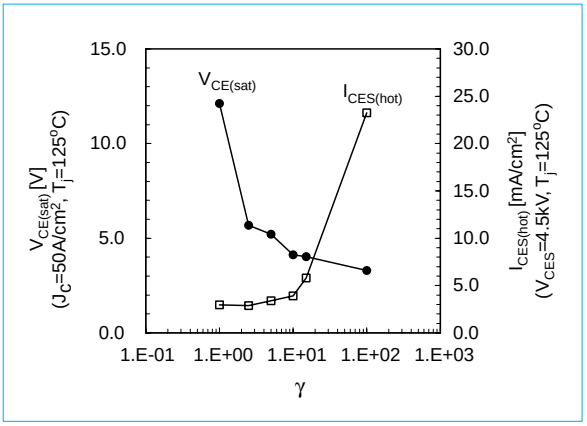

Fig. 4 Dependence of $V_{CE(sat)}$ and $I_{CES(hot)}$ on γ in the 4.5kV-IGBT chip

In order to reduce $I_{CES(hot)}$ still further, investigations were also performed from the aspect of lifetime control, that is, looking at the depth of proton irradiation from the p⁺ collector side.

Fig. 5 shows the dependence of the hot leakage current $I_{CES(hot)}$ and the ratio between the cross-point current and the rated current $I_{ztc}/I_{C(rating)}$, on the depth of proton penetration D_{H+} from the p⁺ collector side. The depth for D_{H+} was selected to be as shallow as possible while still keeping $I_{ztc}/I_{C(rating)}$ to about 0.5. (Note that the cross-point current (I_{ztc}) is the intersection of the curve of $V_{CE(sat)}$ plotted against I_C with the

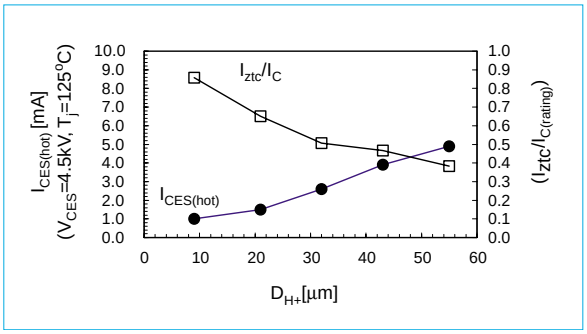

Fig. 5 Dependence of I_{CES} and I_{ztc}/I_C on DH+ in the 4.5kV-IGBT chip

collector current I_C at T_J=25°C and at T_J = 125°C.)

The design described above fulfilled the initial target of $V_{CE(sat)}$ = 3.3V, while still controlling $I_{CES(hot)}$. (Conditions: rated collector current and junction temperature T_J = 125°C) was confirmed in all three of the 4.5kV HVIGBT module products, and was thus selected.

Table 1 gives the absolute maximum ratings and Table 2 the important product characteristics (specification parameters).

Table 1 Maximum Ratings of the 4.5kV HVIGBT Module

Symbol	Item	Conditions	CM400HB-90H	CM600HB-90H	CM900HB-90H	Unit
V_{CES}	Collector-emitter voltage	V_{GE}=0V, T_j=25°C	4500	4500	4500	V
V_{GES}	Gate-emitter voltage	V_{CE}=0V, T_j=25°C	±20	±20	±20	V
I_C	Collector current	T_C=25°C	400	600	900	A
I_{CM}		Pulse	800	1200	1800	A
I_E	Emitter current	T_C=25°C	400	600	900	A
I_{EM}		Pulse	800	1200	1800	A
T_j	Junction temperature	---	-40~+125	-40~+125	-40~+125	°C
T_{stg}	Storage temperature	---	-40~+125	-40~+125	-40~+125	°C
V_{iso}	Isolation voltage	Charged part to base plate, rms sinusoidal, AC60Hz 1min.	6000	6000	6000	V
---	Mounting torque (min.~max.)	Main terminal screw : M8	6.67~13.00	6.67~13.00	6.67~13.00	N·m
		Mounting screw : M6	2.84~6.00	2.84~6.00	2.84~6.00	N·m
		Auxiliary terminal screw : M4	0.88~2.00	0.88~2.00	0.88~2.00	N·m
---	Mass (typ.)	---	1.5	1.5	2.2	kg

Table 2 Key Characteristics of the 4.5kV HVIGBT Module

Symbol	Item	Conditions		CM400HB-90H	CM600HB-90H	CM900HB-90H	Unit
I_{CES}	Collector cutoff current (max.)	V_{CE} : Rated Voltage	T_j=25°C	8	12	18	mA
		V_{GE} : 0V	T_j=125°C	40	60	90	
$V_{GE(th)}$	Gate-emitter threshold voltage (typ.)	I_C : Rated Current/10000 V_{GE}=10V , T_j=25°C		6.0	6.0	6.0	V
I_{GES}	Gate leakage current (max.)	V_{GE}=V_{GES} , V_{CE}=0V		0.5	0.5	0.5	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage (typ.)	I_C : Rated current	T_j=25°C	3.0	3.0	3.0	V
		V_{GE}=15V	T_j=125°C	3.3	3.3	3.3	
V_{EC}	Emitter-collector voltage (typ.)	I_E : Rated current	T_j=25°C	4.0	4.0	4.0	V
		V_{GE}=0V	T_j=125°C	3.6	3.6	3.6	
$R_{th(j-c)Q}$	Thermal resistance (max.)	IGBT part		0.023	0.015	0.010	k/W
$R_{th(j-c)R}$		FWDi part		0.045	0.030	0.020	k/W
$R_{th(c-f)}$	Contact thermal resistance (typ.)	Conductive grease applied		0.015	0.010	0.007	k/W

Because the 4.5kV HVIGBT module was designed, as described above, to minimize the heat generated from the semiconductor chips, this design promises to reduce power loss in systems using these products. They will also contribute to energy conservation when applied to the converters and inverters for use at increasingly higher voltages in the future. ❑

Analysis and Simulation Technologies for High-Reliability Design of Power Modules

*by Toshiyuki Kikunaga and Takeshi Ohi**

High precision analysis and simulation technologies for electrical and thermal phenomena within power semiconductor modules are indispensable if the reliability of the designs of the modules is to be improved. This article will discuss three-dimensional electromagnetic field analysis technologies used in the design of interconnects within power modules, and will discuss electro-thermal simulation technologies that combine models of the electrical circuits in power semiconductor chips with models of the thermal paths in the module structure.

Electromagnetic Field Analysis in the Design of Interconnect Lines in Power Modules

High-capacity power modules are made by connecting a large number of power semiconductor chips, for example, insulated gate bipolar transistors (IGBTs) and free wheeling diodes (FWDs) in parallel within the module. Current imbalances between the respective chips in these modules affect the durability of the module and the uniformity of the thermal distribution within the chips. Because of this, current balancing is important in improving the performance and long-term reliability of the modules.

Mutual inductance in the three-dimensional interconnect systems such as found in electrodes in power modules creates complex linkages between the various interconnect lines. Three-dimensional electromagnetic field analysis is useful in evaluating the current distributions and the impedances in these parallel circuits. The application of this analysis technology makes it possible to design these interconnects based on a quantitative understanding of the electromagnetic linkages and of difference in impedances in the parallel circuits.

Methods of three-dimensional electromagnetic field analyses include the finite element method (FEM), the boundary element method (BEM), and the finite difference time domain (FDTD) methods. Here we used the finite element method (FEM), able to analyze precisely the electromagnetic field, current distribution and impedance for the complex geometries of interconnect conductors in power modules. The analysis results matched closely the experimental results, confirming the usefulness of this method as a design tool.

Fig. 1 is an example of an analysis model for a module. Copper blocks (1) to (4) in the Fig. were used instead of the semiconductor chips in order to isolate the effects of the interconnect impedances in the current distribution characteristics given. The collector terminal and emitter terminal at the top of the module were connected to external parallel plate conductors. The current distribution characteristics were analyzed for the high frequency domain (300kHz) to evaluate the circuit impedance, and for the low-frequency domain (50Hz), where the circuit resistance dominates.

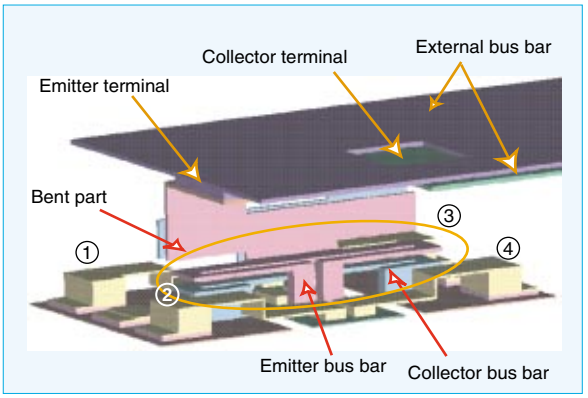

Fig. 1 Three-dimensional electromagnetic analysis model for power modules

Fig. 2 shows the results of the analysis of the current balance between chips. When the frequency was 300kHz, the average electric current on the chip (3) and (4) side was larger than the average electric current on the chip (1) and (2) side. This is due to the difference in the circuit inductance in the left- and right-bent parts of emitter and collector bus bars. In addition, the differences in electric currents in chip (1) and chip (2) and in chip (3) and chip (4), are due to differences in the electric current path. On the other hand, when the frequency was at 50Hz, the differences in the circuit inductances had little effect on the distribution of the electric current, and so only the effect of the differences in the circuit resistance was evident.

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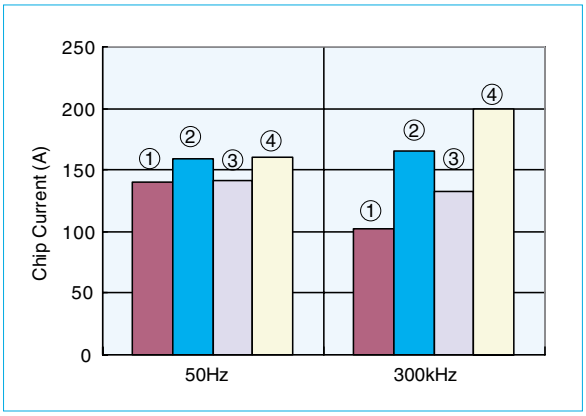


Fig. 2 Analysis of current balance characteristics

In order to evaluate the correctness of the analysis results, the test module that was the basis for creating the analytical model in Fig. 1 was inserted into a half-bridge switching circuit, and the currents were measured for the respective chips. Fig. 3 compares the experimental results with the analytical results. The current imbalance ratios at the current peak for the various chips were compared with those of the analytical results at a high frequency of 300kHz, because the frequency component of the rising electric current in the switching test was about this frequency. The measured results with a DC power supply were compared with the results of the analysis at a low frequency of 50Hz. The experimental results closely matched the analytical ones at both at high and low frequencies.

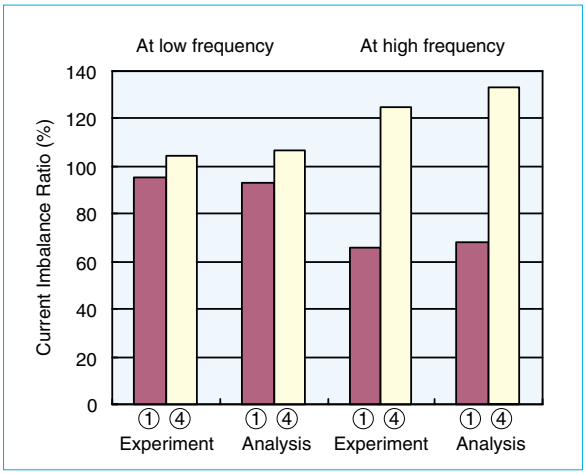


Fig. 3 Comparison of experimental and analytical results for chip current imbalance

The current imbalance caused by unbalanced inductance in the interconnect lines may be more pronounced in the higher-voltage larger-capacity modules, where collector and emitter terminals are further apart and there are more chips in parallel. Thus, this three-dimensional electromagnetic field analysis technology is useful in the designs of such modules. This analysis technology was used in the design to optimize the shapes of the electrodes in a high-voltage intelligent power module (IPM) with a rated voltage of 3300V/1200A, and excellent current balance results were obtained.

Simulation of Temperature Distribution on Semiconductor Chip Surfaces

Generally, wire bonding to the interconnect lines on the surface of the semiconductor chip is used in power modules. In power modules, a number of aluminum wires are bonded onto the power semiconductor chips and the main current flows through these wires. The bond between an aluminum wire and the chip surface suffers heat stress through repeated temperature cycles. This heat stress eventually causes the bonded wire to separate from the surface, a phenomenon that limits the lifetime of power modules. Control of temperature distribution on the chip is therefore very important. Optimizing the disposition of bonds on the chip can reduce temperature swings and minimize the current concentration due to voltage drop along the surface pattern, thereby improving the lifetime and reliability of the power module. Here, electrothermal simulation is presented as a method of evaluating the temperature distribution on a chip; it can provide a method of optimizing the disposition of wire-bonding points so as to reduce chip temperature gradients.

Fig. 4 shows the IGBT chip emitter surface and the electrical circuit model. The emitter electrode is separated into stripes, and in this Fig., aluminum wires are bonded near the middle of each stripe. The electrical circuit model for the IGBT is a circuit model for a single stripe. In order to take into consideration the thermal distribution on the chip and the electrical resistance of the aluminum electrode on the emitter surface, which contribute to the collector current distribution of the chip, each stripe is divided into multiple IGBT segments ($IGBT_0$ to $IGBT_n$) and electrical resistances (R_{A11} to R_{A1n}) corresponding to the resistances of the aluminum electrodes between the respective IGBT emitters were inserted. In addition, the parameters for each IGBT segment circuit models are selected so that the IGBT chips that are represented by the electrical circuit models match the actual measured values for the V-I characteristics of the actual chips.

Fig. 5 shows both the simulation results (the solid line) and the measurement results (marked by circles, inverted triangles, etc.) of the voltage distributions of the various collector currents

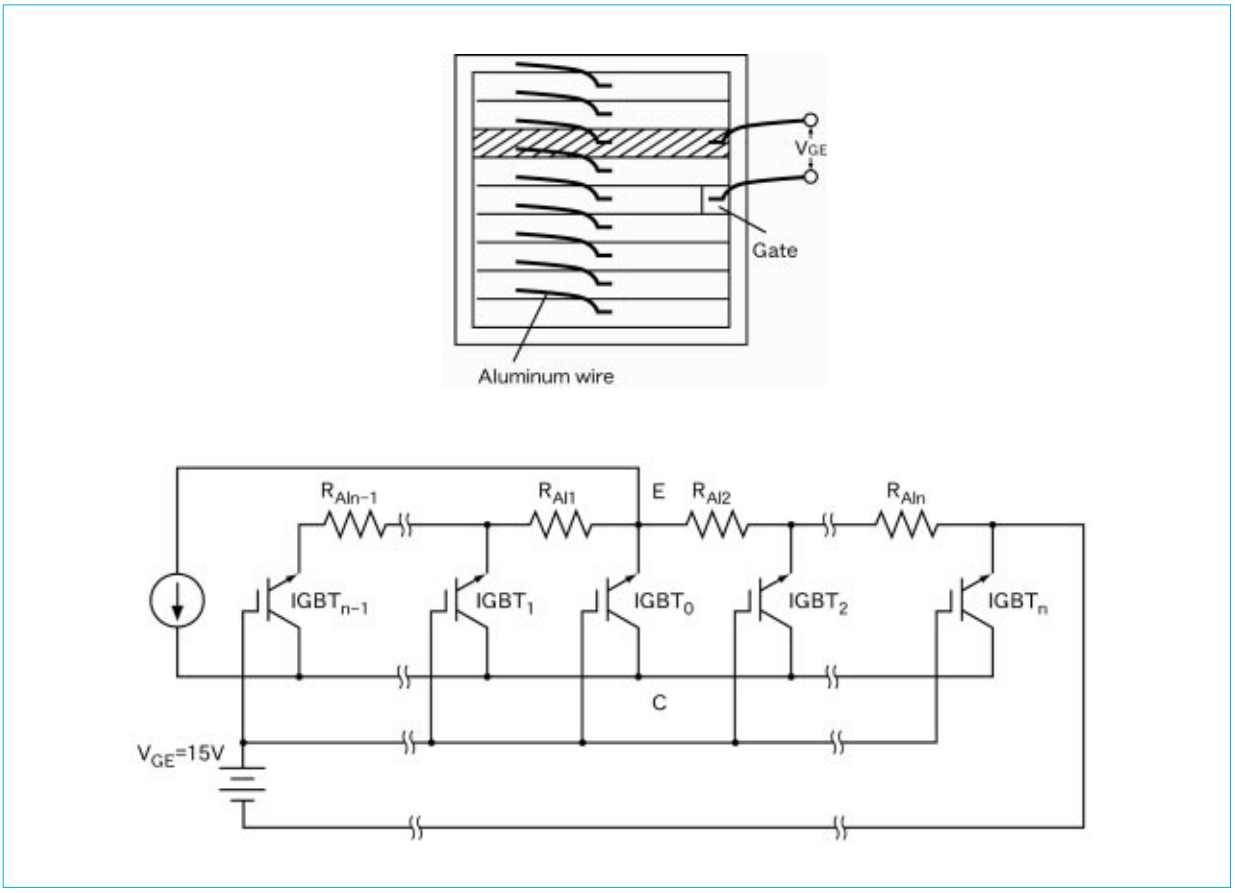


Fig. 4 Emitter surface of IGBT chip and electrical circuit model separating the IGBT chip into small IGBT segments

referenced to the potential of the aluminum wire bond on the emitter electrode surface of one of the stripes. The simulation results matched the measurements quite well, indicating that the electrical circuit models described above were appropriate.

Fig. 6 shows the layered structure of the cross section of a module, including the IGBT chips, the ceramic substrate, the baseplate, and the heat sink, doing so as a network of thermal paths in the electrothermal simulation. The various thermal resistances are calculated from the thermal conductivities and thicknesses of the materials in the structure. This example is a model of the thermal paths for a single chip, and the influence of the adjacent chips is not considered in this model.

The V-I characteristics of the various IGBT segments in the electrical circuit model of Fig. 6, were modeled, taking the temperature dependencies into account. The voltages and currents for the IGBT segments obtained from the static characteristics of the IGBT chip were used to calculate the thermal generation in each of the IGBT segments, the temperature fluctuations were calculated from the thermal path model, and the calculations iterated until the temperature in each of the IGBT segments reached convergence. The losses in the aluminum electrodes on the emitter surfaces and the thermal interference between the IGBT segments within each stripe were taken into consideration, and the cross-wise thermal conduction in the solder parts and grease part in

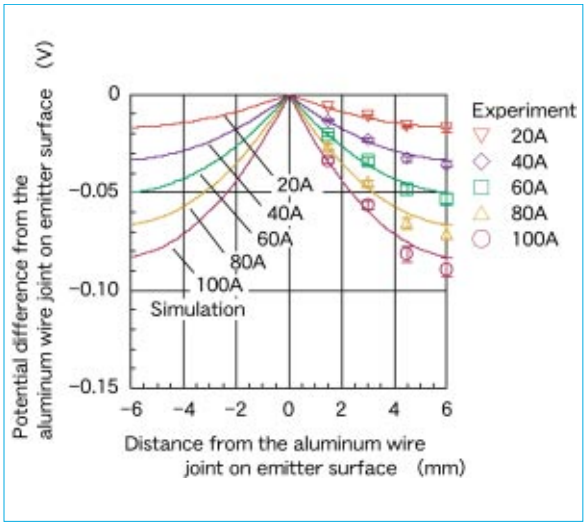


Fig. 5 Simulation results and measurements of potential distribution on the emitter surface.

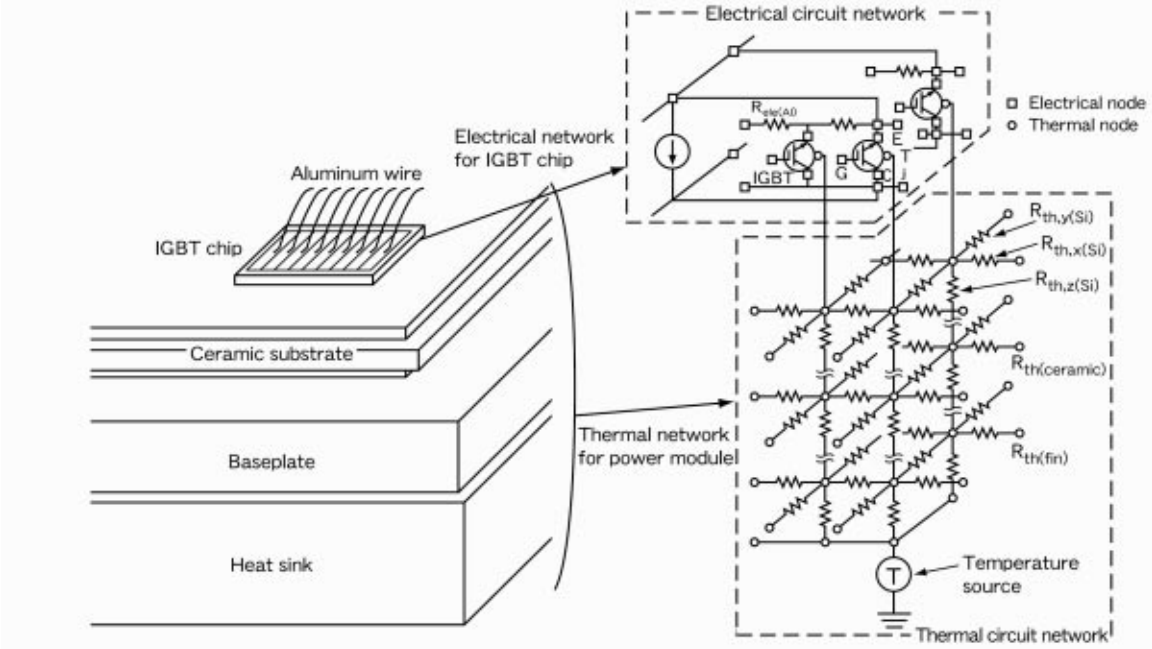
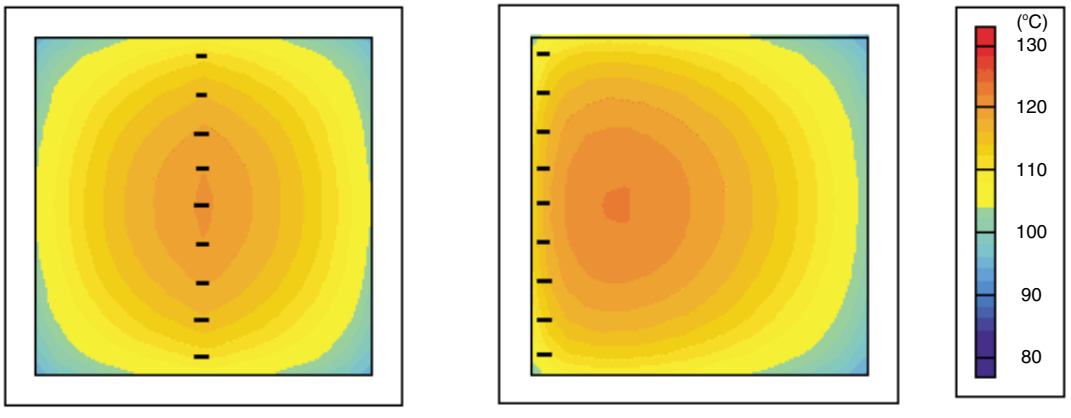


Fig.6 Electrothermal network of an IGBT chip.

the layered structure of the module cross-section was ignored. The heat sink was held at 23ºC, matching the experimental conditions.

Fig. 7 and Fig. 8 show the results of simulations and experiments on the IGBT chip surface temperature distribution when wire bonds have been made to the center parts and peripheral parts of the emitter electrodes (where the black short lines show the positions of the aluminum wire bonds). The collector current was 105A. Power was applied until the temperature distribution on the surface of the chip reached a steady state, and then an infrared camera was used to measure the temperature distribution. It was found that the temperature distributions were nearly identical.

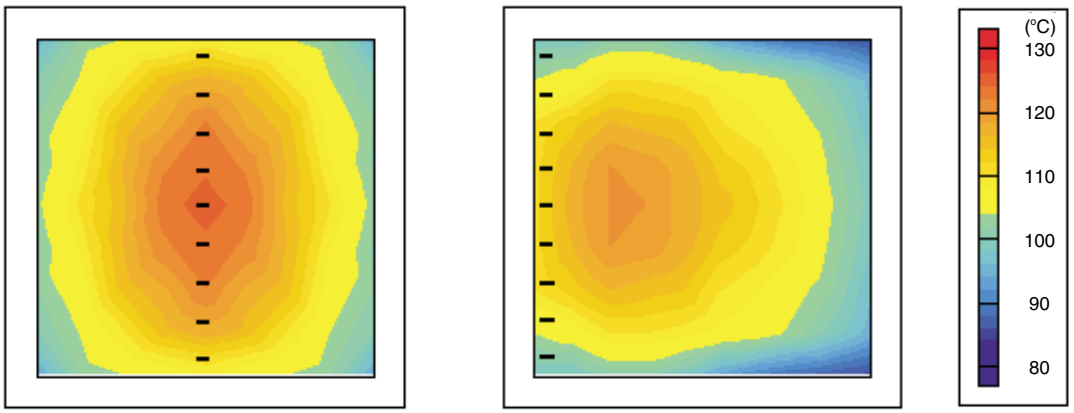
Fig. 9 is the result of a simulation of the temperature distribution, ignoring the temperature dependencies of the electrical characteristics and the electrical resistances of the IGBT chip emitter surface. In other words, the simulation of the thermal distribution assumes uniform



Aluminum wires bonded at the central area of emitter.

Aluminum wires bonded at the periphery of emitter.

Fig. 7 Results of electrothermal simulation of the temperature distribution in an IGBT chip



Aluminum wires are bonded at the central area of emitter.

Aluminum wires are bonded at the periphery of emitter.

Fig. 8 The comparison of measured temperature distributions in IGBT chips with different wire bond positions

losses throughout the chip. The total loss within the chip is essentially the same as the loss shown in Fig. 7, where a wire bond is made at the center of the emitter electrode. The thermal distribution in Fig. 9 is clearly different from the distributions in Figs. 7 and 8. Consequently, it is evident that the assumption of uniform losses is inadequate for accurate evaluations of the temperature distributions on the surface of the chip, and that electrothermal simulations are essential.

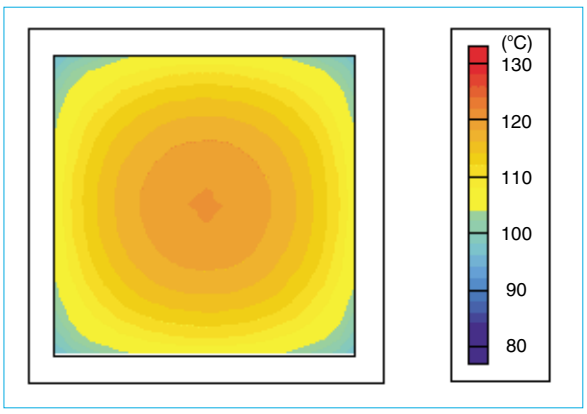


Fig. 9 Results of an electrothermal simulation of the temperature distribution of an IGBT chip, assuming uniform power dissipation

At present, work is proceeding on dynamic simulations of power semiconductor circuits in conjunction with electromagnetic field modeling, and on simulations of transient electro-thermal phenomenon.❑

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Next-Generation IGBTs (CSTBTs)

*by Hideki Takahashi and Yoshifumi Tomomatsu**

Mitsubishi Electric Corporation has announced a carrier stored trench gate bipolar transistor (CSTBT) that has reduced on-state voltages by significant improvements to the carrier distribution in trench IGBTs (TIGBTs). The corporation has developed this CSTBT as its next-generation IGBT. It has demonstrated all of the performance advances hoped for in next-generation power chips. This article describes the results of evaluations of the CSTBT prototypes.

Ever since IGBT modules (used primarily in invertors) were first marketed, new generations of IGBT chips have been produced every few years, steadily improving the performance frontier for the trade-off between switching loss and saturation voltage (an indicator of loss). Until the third generation, improvements resulted from technologies to miniaturize cells, but a revolutionary new structure was introduced in the fourth generation; in addition to further miniaturizing the cells, a trench gate structure was introduced, resulting in a substantial leap in performance.[1]

In response to the needs of a market constantly searching for improvements in energy conservation, the corporation announced its CSTBT in 1996[2], and commenced research and development in both structures and manufacturing processes for these next-generation power chip products.[3]

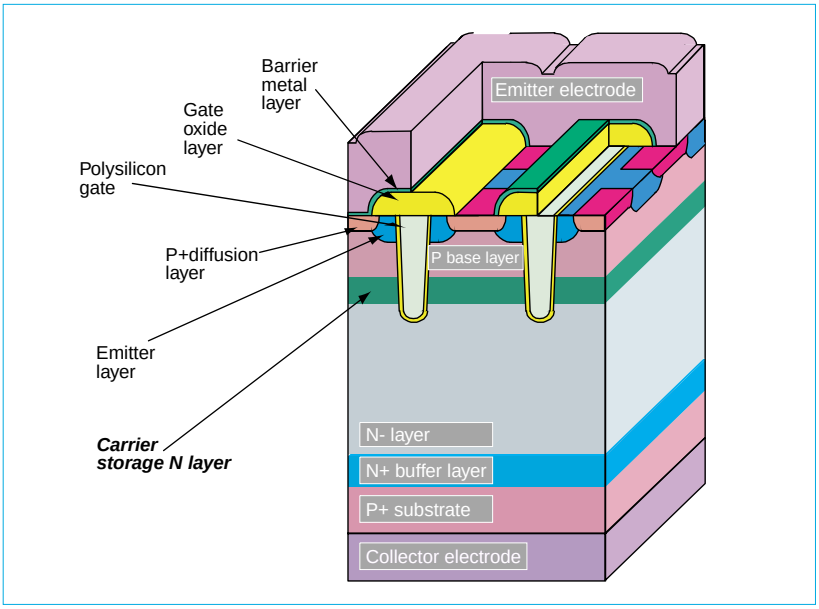

Fig. 1 Three·dimensional view of CSTBT

The Structure and Benefits of CSTBTs

Fig. 1 shows a three-dimensional cross section of a CSTBT. Structurally, the CSTBT is characterized by the addition of an n-type layer with a relatively high impurity density between the p-type base layer and the n- layer in the trench IGBT (TIGBT). When the conventional TIGBT is in an ON state, holes are injected into the n- layer from the p+ layer on the collector side, and these holes pass to the emitter side. On the other hand, in the CSTBT, the impurity density of the n layer that forms a junction with the p base is greater than for the n- layer, so the junction voltage at the junction between the p base and the n layer is greater than the junction voltage at the junction between the p base and the n- layer in the TIGBT. This high junction voltage becomes a barrier preventing the holes that were injected into the n- layer from the p+ layer from passing into the emitter side. In other words, the n layer causes the holes to accumulate within the element by restricting the movement of the holes to the p base layer. This charge accumulation function causes the ON voltage for the CSTBT to be substantially lower than for the TIGBT.

Performance of the 600-volt CSTBT

To confirm the superior properties of the CSTBT, a CSTBT chip was prototyped and evaluated using the same wafers and the same 1µm design rule as for the TIGBT. The CSTBT had a reverse bias voltage of 600V and a current-carrying capacity of 50A. Because, in the CSTBT, the primary junctions were formed with an n-type layer with a relatively high impurity density in order to store the carriers, it was more difficult to ensure reverse-bias voltage capabilities than it

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was for the TIGBT; however, the reverse bias voltage was successfully secured by optimizing both the thickness and the impurity density of the carrier storage layer, and by using high precision control. Fig. 2 shows the waveforms for the current and the voltage when the CSTBT is OFF. As is clear from the figure, the CSTBT rated at 600V has a 720V reverse bias capability, so there is adequate margin above the rated voltage.

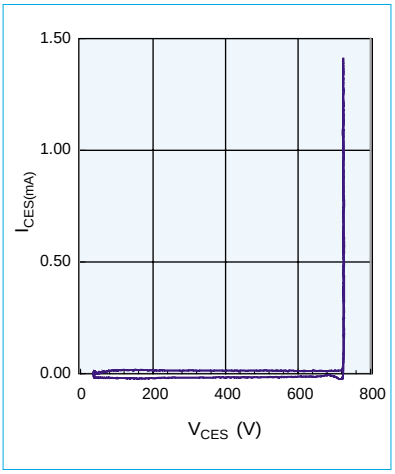

Fig. 2 Breakdown voltage of CSTBT.

Fig. 3 shows the output characteristics of a CSTBT exposed to electron-beam radiation in the same way as a TIGBT is exposed (in order to control the minority carrier lifetime). The output characteristics are shown at both 25°C and 125°C. The

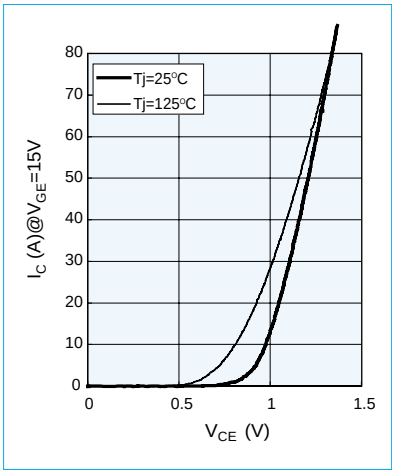

Fig. 3 I·V characteristics of CSTBT.

saturation voltage at the rated current ($V_{CE(sat)}$) was 1.22V at T_J=25°C, and 1.15V at T_J=125°C, 0.3 to 0.4V less than the conventional TIGBT.

Fig. 4 is a curve showing the tradeoffs between the switch-off loss, $E_{SW(off)}$ and the $V_{CE(sat)}$. As described above, the CSTBT is superior to the TIBGT in terms of its ON characteristics, and thus the CSTBT tradeoff curve is about 0.4V better than the TIGBT for the same switching loss. When it comes to this tradeoff relationship between the $V_{CE(sat)}$ and the $E_{SW(off)}$ the CSTBT is superior to any other MOS gate device so far announced for applications at 600V.

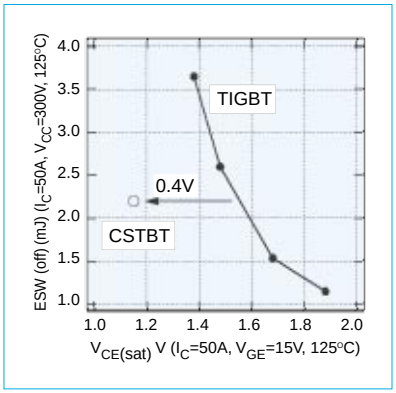

Fig. 4 Trade·off relationship between on·state voltage drop and turn·off loss for both CSTBT and TIGBT.

It was also confirmed that the reverse bias safe operation area (RBSOA) could perform turn-off switching at 500A (a current density of 2100A/cm^2), ten times the rated current.

As described above, the CSTBT proposed by Mitsubishi Electric is positioned as the next-generation power chip after the TIGBT, and, as a step in this direction, the corporation has developed technologies for insuring reverse biasing capabilities and has established design technologies for carrier storage layers, validating the performance of the 600V/50A CSTBT. As a result, the CSTBT has been able to improve the tradeoff relationship between the $V_{CE(sat)}$ and the E_{OFF} by about 0.4V over the conventional TIGBTs without incurring any loss in performance in terms of the switching time or reverse bias voltage. This tradeoff relationship is the best of any MOS gate element announced to date for 600V or above.

Development efforts are underway on high-performance module products using the CSTBT chips in order to contribute to the market looking for improved energy conservation. ❑

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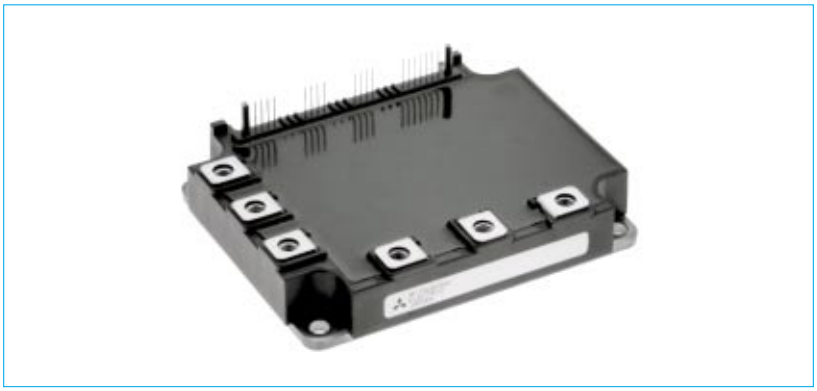
Fourth Generation IPM, "S-DASH Series"

Given the improvement in performance of power modules, the market now has a new set of demands applying to power modules in addition to its conventional demands for high performance, compact size, and low losses. These new demands include greater ease of use and environmental friendliness. To meet these needs, Mitsubishi Electric Corporation has released its fourth-generation intelligent power module (IPM) the "S-DASH Series," in order to reduce the saturation voltage and reduce electromagnetic noise.



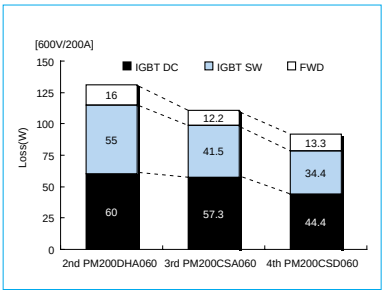
The S-DASH intelligent power module

Applications

Ideal for compact inverter servos and other motor-controlled equipment for AC 220V and AC 440V applications, and for compact inverters in UPS equipment and other power-supply equipment.

Features

1. Reduced losses through the use of the fourth-generation 1-µm design rule planar insulated gate bipolar-transistor chip.
2. Improved recovery characteristics and reduced electromagnetic noise through the use of a newly designed free-wheeling diode.
3. Maintains package compatibility with the corporation's second- and third-generation intelligent power modules.
4. Built-in fault-signaling outputs for over-current, short circuits, over-temperature and drive supply under-voltage. ❑



A comparison of the losses in each generation of the Mitsubishi Electric Corporation intelligent power modules.

SiC Element Technology

Power devices are used broadly in home electronics, industrial applications, electric trains, and electric power generation and transmission. These power devices contain switching elements equipped with control electrodes (typically insulated gate bipolar transistors), along with diodes to provide the rectifying function.

When compared to silicon (Si), silicon carbide (SiC) devices have superior physical characteristics, suggesting that SiC will be the next generation of semiconductor materials to transcend the physical limitations of silicon in power devices requiring higher blocking voltages and lower ON resistances. As a result SiC has increasingly become the focus of research.

Of greatest interest to device manufacturers is that SiC has ten times the dielectric breakdown electric field strength of silicon, meaning that the high-resistance layer need only be one-tenth the thickness to maintain the same high voltages. Because it is also possible to increase the substrate electron density by a factor of 100, the use of SiC can reduce the ON resistance to one-thousandth that of silicon in comparable unipolar structures. In other words, in a class of devices with blocking voltages of the order of 1kV or higher, the use of SiC enables unipolar structures such as field-effect transistors and Schottky barrier diodes, where conventionally bipolar structures have been required to reduce the ON resistance when silicon was used. This is expected to resolve the problems that occur in bipolar structures when performing high-speed switching.

In diode technology, a Schottky barrier-type diode rated at 600V and several amperes was released at the beginning of 2001. In fields requiring higher blocking voltages (several kVs), there have been announcements relating to recovery performance and reliability testing results in bipolar structures, indicating that the release of such structures may be imminent.

The most intense research, however, is in the field of voltage-driving field-effect transistors (FETs) as switching elements. Aggressive efforts are currently being made to bring to market structures wherein, for example, the resistance of the channel layer is reduced and this layer is fabricated somewhat more deeply buried in the substrate below the surface itself.

Remarkable progess has been made in crystal technologies since 1993, due to burgeoning demand for light-emitting diodes, and advanced firms in the United States have now been joined by substrate manufacturers in Europe and Japan. The issues faced in bringing this technology to market include reducing defects and increasing diameters. The density of defects known as "micropipes," with diameters of several µm, has reached the 1.1 defect/cm^2 level, and discussion has started regarding the effects of, for example, dislocation defects. As for increased diameters, some crystal manufacturers have indicated that they will begin sales of four-inch substrates in the next few years.

Mitsubishi Electric Corporation began technical research in this MITI-designated critical region in June 1994, and since 1998 it has participated in the MITI super-low loss electrical element development process, engaging in research into and development of MOSFETs. ❑

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